LEGAL NOTICES

THIS DOCUMENT CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION OF FOCUS ENHANCEMENTS AND ITS RECEIPT OR POSSESSION DOES NOT CONVEY ANY RIGHTS TO REPRODUCE OR DISCLOSE ITS CONTENTS, OR TO MANUFACTURE, USE, OR SELL ANYTHING THAT IT MAY DESCRIBE.

REPRODUCTION, DISCLOSURE, OR USE IN WHOLE OR IN PART WITHOUT THE SPECIFIC WRITTEN AUTHORIZATION OF FOCUS ENHANCEMENTS IS STRICTLY FORBIDDEN.

EVERY EFFORT HAS BEEN MADE TO ENSURE THAT THE INFORMATION IN THIS DOCUMENT IS COMPLETE AND ACCURATE AT THE TIME OF PRINTING; HOWEVER, THE INFORMATION CONTAINED IN THIS DOCUMENT IS SUBJECT TO CHANGE.

FOCUS ENHANCEMENTS CANNOT BE RESPONSIBLE FOR UNAUTHORIZED USE OF EQUIPMENT AND WILL NOT MAKE ALLOWANCE OR CREDIT FOR UNAUTHORIZED USE OR ACCESS

Macrovision Product Notice

The FS472 and FS474 are protected by U.S. patent numbers 5,583,936; 6,516,132; 6,836,549; and 7,050,698 and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited. FS472 and FS474 devices can only be sold or distributed to Macrovision Authorized Buyers.

Revision History

Date	Revision	Description
March 2008	1.2	New Datasheet format. Updated “Product Features”. Added address locations for all reserved registers. Updated Figure 2 “MUX Mode Timing Example”. Fixed text in Figure 1 “ Non-MUX Mode Timing Example”. Updated bit description for registers 0x40 and 0x42.
Nov 2007	1.1	Corrected text on page 10. Clarified register description (section 2.2.40). Paragraph 2.2.99 changed to "Reserved". Functionality not supported.
Nov 2007	1.00	Datasheet Released.
May 2007	0.95	Preliminary Datasheet Released.

Contact Information

Email: support@FOCUSSEMI.com
Phone: (503) 615-7700
Fax: (503) 615-4232

MAIL: FOCUS ENHANCEMENTS, Inc.
22867 NW Bennett St., Suite 200
Hillsboro, OR 97124 USA

Note: *This page intentionally left blank.*

TABLE OF CONTENTS

Note: *This page intentionally left blank.*

1.0 Document Overview

To make specialized information easier to find, hardware/software/firmware information is organized into separate documents. Each document addresses a different purpose or user.

- This document, the FS471, FS472, FS473 and FS474 Software/Firmware Datasheet, is for programmers. It provides information on programming the FS471, FS472, FS473 and FS474.
- The FS471, FS472, FS473 and FS474 Product Brief provides general information for all users.
- The FS471, FS472, FS473 and FS474 Hardware Datasheet is for system designers. It provides information on developing FS471, FS472, FS473 and FS474 applications.

Throughout this document FS471 is used as a general term to reference the FS471, FS472, FS473 and FS474. The FS472 and FS474 support Macrovision anti-copy protection, while the FS471 and FS473 do not.

Table 1.1 lists a general overview of the differences between the FS471, FS472, FS473, and FS474.

Table 1.1 Part Number Description

Order Number	Temperature Range	Screening	Package	Product
444-2151LF	0°C to 70°C	Commercial	80-ball FBGA	FS471 - Tape & Real
444-2152LF	0°C to 70°C	Commercial	80-ball FBGA	FS472 - Tape & Real
444-2153LF	0°C to 70°C	Commercial	100-pin TQFP	FS473 - Tape & Real
444-2154LF	0°C to 70°C	Commercial	100-pin TQFP	FS474 - Tape & Real

1.1 Acronym List

Acronym	Description	Acronym	Description
BGA	Ball Grid Array	BIST	Built In Self Test
BLU	BLUe	CR	Command Register
DAC	Digital to Analog Converter	DLY	DeLaY
DTV	Digital TeleVision	ENC	Encoder
FAE	Field Applications Engineer	FF	Flicker Filter
FIFO	First In First Out	FLD	FieLD
FLK	FLicKer	GPIO	General Purpose Input Output
GRN	GReeN	HDSC	Horizontal Down SCaler
HSYNC	Horizontal SYNC	HUSC	Horizontal Up SCaler
ID	Identifier	IHW	Input Horizontal Width
IHO	Input Horizontal Offset	INV	INVerter
I/O	Input/Output	IVO	Input Vertical Offset
LAT	LATency	MISC	MISCellaneous
MV	MacroVision	NTSC	National Television System(s) Committee (North American TV Standard)
PAL	Phase Alternating Line (European TV Standard)	PLL	Phase Locked Loop
PWR	PoWer	RTCD	RaTe Converter Denominator
RTCN	RaTe Converter Numerator	R/W	Read/Write
SDFT	Special Derived Field Timing	SDTV	Standard Definition TeleVision
SHP	Sharpness	SD	Standard Definition
TBD	To Be Determined	TLA	Three Line Average
UIM	Universal Input Matrix	VSC	Vertical Scaling Coefficient
VSYNC	Vertical SYNC	WSS	Wide Screen Signaling

1.2 Document Organization

This document provides information necessary for programming or developing driver software for the FS471, FS472, FS473 and FS474 TV encoders. It is divided into the following sections:

- Document Overview: lists FS471 reference documents and acronyms that are used through this datasheet as well as how this document is organized.
- Control Register Definitions:
- Control Register Map - lists the FS471 control register map
- Control Register Definitions - defines the FS471 control registers.

2.0 Control Register Definitions

2.1 Control Register Map

The general function labels of the FS471 registers are intended to help design engineers determine which registers affect the following specific functions of the FS471:

- SDTV Input - settings to the FS471 inputs in SDTV applications
- SDTV Output - FS471 SDTV output settings
- Control - FS471 control parameters
- Clock - FS471 clock settings
- Color Matrix - FS471 input color conversion matrices

Table 2.1 Register References

General Function	Name	Offset	Default Value
SDTV Input	I2C_IHO – Input Horizontal Offset	0x00	64d
SDTV Input	I2C_IVO – Input Vertical Offset	0x02	3d
SDTV Input	I2C_IHW – Input Horizontal Width	0x04	720d
SDTV Input	I2C_VSC – Vertical Scaling Coefficient	0x06	0d
SDTV Input	I2C_VSC 2 – Vertical Scaling Coefficient	0x08	0d
SDTV Input	I2C_HSC – Horizontal Down/Up Scaling	0x0A	0d
Control	I2C_CR – Command Register	0x0C	0x4000
Control	I2C_MISC1 - Miscellaneous Bits	0x0E	0x8003
Control	I2C_MISC2 - Miscellaneous Bits Register 2	0x10	0x0000
Clock	I2C_RTCNL – Numerator of Rate Converter (Low)	0x12	0x2B7D
Clock	I2C_RTCNH – Numerator of Rate Converter (High)	0x14	0x0048
Clock	I2C_RTCDL– Denominator of Rate Converter (Low)	0x16	0x2B7D
Clock	I2C_RTCDH – Denominator of Rate Converter (High)	0x18	0x0048
Clock	I2C_HWIDTH – Horizontal Width	0x1A	858d
Clock	I2C_HSYNCS – Horizontal Sync Start	0x1C	74d
Clock	I2C_HSYNCE – Horizontal Sync End	0x1E	138d
SDTV Output	I2C_SHP – Flicker Filter Sharpness	0x20	0d
SDTV Output	I2C_FLK – Flicker Filter Coefficient	0x22	12d
Control	I2C_GPIO - General Purpose Input Outputs	0x24	0d
N/A	Not Accessible	0x26	N/A
N/A	Not Accessible	0x28	N/A
N/A	Not Accessible	0x2A	N/A
N/A	Not Accessible	0x2C	N/A
Control	I2C_PART - Part Identification Number	0x2E	0xFE07
Control	I2C_SP – Status Port	0x30	0x0000
Control	I2C_FFO – FIFO Status Port	0x32	0x0000
SDTV input	I2C_FFO_LAT – FIFO Latency	0x34	130d
SDTV Output	I2C_VWIDTH – Vertical Width	0x36	525d
SDTV Output	I2C_VSYNCS – Vertical Sync Start	0x38	42d
SDTV Output	I2C_VSYNCE – Vertical Sync End	0x3A	45d
SDTV Output	I2C_VID_CNTL0 – Video Control 0	0x3C	0x0000
SDTV Output	I2C_FLD_DLY – Field Delay Value	0x3E	0x0000
SDTV Output	ENC_CHR_FREQ0 – Chroma Sub-Carrier Frequency Low	0x40	0x7C1F
SDTV Output	ENC_CHR_FREQ2 – Chroma Sub-Carrier Frequency High	0x42	0x21F0
SDTV Output	ENC_CHR_PHASE – Chroma Phase	0x44	0x0000
SDTV Output	ENC_MISC - Encoder Miscellaneous Registers 0 and 1	0x46	0x0900
SDTV Output	ENC_RGB_YUV - Chroma Gain and Bandwidth Control	0x48	0x0000
SDTV Output	ENC_HSYNC_W – Horizontal Sync Width	0x4A	63d
SDTV Output	ENC_BRST_W – Burst Width	0x4C	68d

General Function	Name	Offset	Default Value
SDTV Output	ENC_BP_LOC – Back Porch Width	0x4E	59d
SDTV Output	ENC_CB_B_LVL - Cr, Cb Burst Amplitude	0x50	59d
SDTV Output	ENC_SLV_CNTL Encoder Slave Control	0x52	0x0000
SDTV Output	ENC_BLACK_LVLL – Black Level	0x54	70d, 02d
SDTV Output	ENC_BLANK-LVLL – Blank Level	0x56	60d, 00d
SDTV Output	Reserved	0x58	N/A
SDTV Output	Reserved	0x5A	N/A
SDTV Output	Reserved	0x5C	N/A
SDTV Output	ENC_NUM_LINEL – Number of Lines	0x5E	131d, 1d
SDTV Output	Reserved	0x60	N/A
SDTV Output	Reserved	0x62	N/A
SDTV Output	ENC_WHITE_LVLL – White Level	0x64	200d, 0d
SDTV Output	ENC_CB_GAIN - Cr, Cb Color Saturation	0x66	137d, 137d
SDTV Output	Reserved	0x68	N/A
SDTV Output	ENC_TINT – Tint Adjustment	0x6A	0x0000
SDTV Output	Reserved	0x6C	N/A
SDTV Output	Reserved	0x6E	N/A
SDTV Output	ENC_BRZ_WAY – Width of Breezeway, Front Porch	0x70	0x1016
SDTV Output	Reserved	0x72	N/A
SDTV Output	Reserved	0x74	N/A
SDTV Output	Reserved	0x76	N/A
SDTV Output	ENC_ACT_LINEL – Active Video Line Pixels	0x78	180d, 0d
SDTV Output	ENC_VLINE_1 – First Video Line	0x7A	0x0015
SDTV Output	ENC_SFT_RST, ENC_VER – Encoder Soft Reset, Encoder Version	0x7C	0x2000
SDTV Output	ENC_UV_STUFF - Miscellaneous	0x7E	0x0002
SDTV Output	ENC_SYNC_LVL – Sync Level	0x80	0x0048
SDTV Output	Reserved	0x82	N/A
SDTV Output	Reserved	0x84	N/A
SDTV Output	Reserved	0x86	N/A
SDTV Output	ENC_VBIBL_LVL – VBI Blank Level	0x88	0x4A00
SDTV Output	ENC_WSS – Wide Screen Signaling	0x8A	0x0007
SDTV Output	ENC_WSS_CLKL – WSS Clock	0x8C	0x2F07
SDTV Output	ENC_WSS_DF1L – WSS Data Field 1 Low	0x8E	0x0000
SDTV Output	ENC_WSS_DF1H – WSS Data Field 1 High	0x90	0x0000
SDTV Output	ENC_WSS_DF0L – WSS Data Field 0 Low	0x92	0x0000
SDTV Output	ENC_WSS_DF0H – WSS Data Field 0 High	0x94	0x0000
SDTV Output	ENC_WSS_LF0 – Field 0 & Field 1 Line Number	0x96	0x0000
SDTV Output	ENC_WSS_LVLL – WSS Level	0x98	0xFF03
SDTV Output	ENC_NOTCH – Encoder Notch	0x9A	0x0000
SDTV Output	I2C_DAC_LD_VAL – DAC Load Value	0x9C	0x0000
SDTV Output	I2C_DAC_LD_DET_REF – Load Detect Parameters	0x9E	0x0000
SDTV Output	I2C_DAC_CNTL – DAC Control Parameters	0xA0	0x0000

General Function	Name	Offset	Default Value
Color Matrix	I2C_RED_MATRIX_COEF – RGB to YCrCb Red Coefficient	0xA2	0x004D
Color Matrix	I2C_GRN_MATRIX_COEF – RGB to YCrCb Green Coefficient	0xA4	0x0096
Color Matrix	I2C_BLU_MATRIX _COEF – RGB to YCrCb Blue Coefficient	0xA6	0x001D
Color Matrix	I2C_RV_SCALE_COEF – RGB to YCrCb Red Scaling Coefficient	0xA8	0x00A0
Color Matrix	I2C_GY_SCALE_COEF – RGB to YCrCb Green Scaling Coefficient	0xAA	0x00DB
Color Matrix	I2C_BU_SCALE_COEF – RGB to YCrCb Blue Scaling Coefficient	0xAC	0x007E
SDTV Output	I2C_CC_DATA_F1 – Closed Caption Field 1 Data	0xAE	0x0000
SDTV Output	I2C_CC_DATA_F2 – Closed Caption Field 2 Data	0xB0	0x0000
SDTV Output	I2C_CC_CNTL – Closed Caption Control	0xB2	0x0000
SDTV Output	I2C_CC_BLNK – Closed Caption Blanking Value	0xB4	0x0000
SDTV Output	I2C_CC_SHT – Closed Caption Blanking Sample	0xB6	0x00F0
N/A	Not Accessible	0xB8	N/A
N/A	Not Accessible	0xBA	N/A
N/A	Not Accessible	0xBC	N/A
N/A	Not Accessible	0xBE	N/A
N/A	Not Accessible	0xC0	N/A
SDTV Output	I2C_LUMA_BW_COEF – Luma Bandwidth	0xC2	0x0000
N/A	Reserved	0xC4	N/A
Clock	I2C_PDIV – PLL Pre-Divider	0xC6	0x0114
Clock	I2C_PLL_AMP – PLL AMP - Main PLL Divider	0xC8	0x012C
Clock	I2C_PLL_VGA – PLL VGA Clock Post Divider	0xCA	0x0003
Clock	I2C_PLL_TV – TV Clock Post Divider	0xCC	0x0003
Clock	I2C_PLL_GCC – PLL GCC Clock Post Divider	0xCE	0x0003
Control	I2C_BYP – Bypass Register	0xD0	0x000A
N/A	Reserved	0xD2	N/A
Control	I2C_PWR_MGMT – Power Management	0xD4	0x0002
SDTV Input	I2C_SDFTH - Special Derived Field Timing - Horizontal	0xD6	0x0114
SDTV Input	I2C_SDFTV - Special Derived Field Timing - Vertical	0xD8	0x0001
N/A	Reserved	0xEA	N/A
N/A	Reserved	0xEC	N/A
N/A	Reserved	0xEE	N/A
N/A	Reserved	0xF0	N/A
N/A	Reserved	0xF2	N/A
N/A	Reserved	0xF4	N/A
N/A	Reserved	0xF6	N/A
N/A	Reserved	0xF8	N/A

2.2 Control Register Definitions

The following definitions are defined as:

- Range - {min value: [max value]}.
- Bits marked as Not Accessible indicate that writing values to these locations have no affect on normal operation.
- Bits market as Reserved indicate that writes to these registers might impact performance. Changes to these registers should be performed as Read, Modify Write functions where only the target bits are changed during a write operation.

2.2.1 I2C_IHO - Input Horizontal Offset (0x00)

- Address Offset - 0x00
- Default Value - 64d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: [Htotal]-1}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	IHO_{10}	IHO_9	IHO_8	IHO_7	IHO_6	IHO_5	IHO_4	IHO_3	IHO_2	IHO_1	IHO_0

Bits	Name	Description
10:0	IHO	**Input Horizontal Offset Bits [10:0].** Horizontal video displacement in pixels (VGA clocks) from leading edge of HSYNC to active video data (0-2047). IHO is an unsigned number. Increasing IHO moves image left. Divide by two in decimation mode.
15:11	Not Accessible	Not accessible (set to 0x0)

2.2.2 I2C_IVO - Input Vertical Offset (0x02)

- Address Offset - 0x02
- Default Value - 3d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: [Total Lines]-1}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	IVO_{10}	IVO_9	IVO_8	IVO_7	IVO_6	IVO_5	IVO_4	IVO_3	IVO_2	IVO_1	IVO_0

Bits	Name	Description
10:0	IVO	**Input Vertical Offset Bits [10:0].** Vertical video displacement in lines from the leading edge of VSYNC to active video data. IVO is an unsigned number. Increasing IVO moves image up.
15:11	Not Accessible	Not accessible (set to 0x0)

2.2.3 I2C_IHW - Input Horizontal Width (0x04)

- Address Offset - 0x04
- Default Value - 720d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: 1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	IHW_9	IHW_8	IHW_7	IHW_6	IHW_5	IHW_4	IHW_3	IHW_2	IHW_1	IHW_0

Bits	Name	Description
9:0	IHW	**Input Horizontal Width [9:0].** Total number of active VGA pixels per line. Video inputs with more than 970 lines require decimation. Divide by two in decimation mode. IHW is an unsigned number. Must be even in down scaling for cache module.
15:10	Not Accessible	Not accessible (set to 0x0)

2.2.4 I2C_VSC - Vertical Scaling Coefficient (0x06)

- Address Offset - 0x06
- Default Value - 0d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {[-32,768]:196,607} equates to 0.5 through 3.99999

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSC_{15}	VSC_{14}	VSC_{13}	VSC_{12}	VSC11	VSC_{10}	VSC_9	VSC_8	VSC_7	VSC_6	VSC_5	VSC_4	VSC_3	VSC_2	VSC_1	VSC_0

Bits	Name	Description
15:0	VSC	**Vertical Scaling Coefficient Bits [18:0].** Vertical scaling factor = (1 + (VSC2:VSC)/65,536). VSC2:VSC is a two's complement number. VSC2 is concatenated with VSC to create a signed 19-bit value.

2.2.5 I2C_VSC_2 - Vertical Scaling Coefficient 2 (0x08)

- Address Offset - 0x08
- Default Value - 0d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {[-32,768]:196,607} equates to 0.5 through 3.99999

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	VSC_2 [VSC_{18}]	VSC_1 [VSC_{17}]	VSC_0 [VSC_{16}]

Bits	Name	Description
2:0	VSC2[2:0) VSC[18:16]	**Vertical Scaling Coefficient 2 Bits [2:0].** Vertical scaling factor = (1 + (VSC2:VSC)/65,536). VSC2:VSC is a two's complement number. VSC2 is concatenated with VSC to create a signed 19 bit value.
15:3	Not Accessible	Not accessible (set to 0x0)

2.2.6 I2C_HDSC/HUSC - Horizontal Down/Up Scaling Coefficients (0x0A)

- Address Offset - 0x0A
- Default Value - 0d
- Attribute - R/W
- Size - 16 bits
- HDSC Allowed Range - {(-63):0} equates to an HDSC factor of 0.74 through 1. Use decimation for 0.73 scaling and below.
- HUSC Allowed Range - {0:127} equates to an HUSC factor of 1 through 1.99. 2-3.99 set with MISC (0E) register (*HUS_DBL_EN*).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$HUSC_7$	$HUSC_6$	$HUSC_5$	$HUSC_4$	$HUSC_3$	$HUSC_2$	$HUSC_1$	$HUSC_0$	$HDSC_7$	$HDSC_6$	$HDSC_5$	$HDSC_4$	$HDSC_3$	$HDSC_2$	$HDSC_1$	$HDSC_0$

Bits	Name	Description
7:0	HDSC[7:0]	**Horizontal Down Scaling Coefficient bits [7:0].** HDSC factor = (1 + HDSC / 128). HDSC is a two's complement number. If HDSC = is non-negative then the image is not affected. Decimation is accomplished along with bit 7 of the MISC register (0x0E). **Note:** To accomplish a scaling factor of 0.26 to 0.5, the Decimator bit (bit 7 of the I2C_MISC register at offset 0x0E) must be set. For example, for a scaling factor of 0.26, set bit 7 of the I2C_MISC register and then program HDSC to -0.63. Note that an even HTotal is required when down scaling.
15:8	HUSC[7:0)	**Horizontal Up Scaling Coefficient bits [7:0].** HUSC factor = (1 + HUSC / 128). HUSC is a two's complement number. If HUSC = is zero or a negative number, then the image is not affected. **Note:** Scale factor of 2 - 3.99 is accomplished by setting bit 14 of the I2C_MISC register at offset 0x0E. For example, a factor of two is achieved by setting bit 14 of I2C_MISC register and programing HUSC to zero. Refer to bypass register, paragraph 3.2.106, for the required settings.

2.2.7 I2C_CR - Command Register (0x0C)

- Address Offset - 0x0C
- Default Value - 0x400
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	P656_OUT	PAL_NTSC	SYNC_MS	FFO_CLR	CACQ_CLR	CDEC_BYP	Not Accessible	Not Accessible	Not Accessible	SRESET

Bits	Name	Description
0	SRESET	**Soft Reset.** Resets the internal state registers to a known state, but does not reset the programmable registers (registers programmed via I2C). **Note:** It is recommended that this reset be asserted for a minimum of 20 OSC_CLK cycles.
3:1	Not Accessible	Not accessible (set to 0x0).
4	CDEC_BYP	**Chroma Decimator Bypass.** Bypass the 4:4:4 to 4:2:2 chrominance decimator for YCrCb 4:2:2 inputs.
5	CACQ_CLR	**Counter Acquisition Flag Clear.** Setting this bit clears the counter acquisition flag, causing the TV domain timing generator to reacquire.
6	FFO_CLR	**FIFO Clear.** Setting this bit clears the FIFO depth registers and the FIFO state register.
7	SYNC_MS	**Sync Master or Slave.** When set, FS471 outputs HSync and VSync to the GCC, otherwise syncs are accepted from the GCC. When set GCC Clock is sourced from the VGA post PLL clock divider, otherwise sourced from the GCC post PLL clock divider (Refer to Figure 5.
8	PAL_NTSC	**PAL or NTSC Input.** Sets the number of lines written through the FIFO and SDFT circuitry. When set, the number of lines is 576 for PAL, when clear, 487 lines for NTSC.
9	P656_OUT	**BT656 Out.** Set to output BT656 through GPIO port. Clear to disable.
15:10	Not Accessible	Not accessible (set to 0x0).

Table 2.2 Pixel Port (P Port) BT.656 Connections

P Port P_FIELD	Input	Output P656_CLK
GPI08	X	PQF
GPIO7	X	V656_7
GPIO6	X	V656_6
GPIO5	X	V656_5
GPIO4	X	V656_4
GPIO3	X	V656_3
GPIO2	X	V656_2
GPIO1	X	V656_1
GPIO0	X	V656_0

2.2.8 I2C_MISC - Miscellaneous Bits (0x0E)

- Address Offset - 0x0E
- Default Value - 0x000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	HUS_DBL_EN	TV_SHORT_FLD	UIM_E	Reserved	BRDG_SYNC	UIM_SDFT	UV_SWAP	UIM_DEC_EN	Reserved	UIM_CCLK	UIM_DCLK	UIM_MOD_3	UIM_MOD_2	UIM_MOD_1	UIM_MOD_0

Bits	Name	Description
3:0	UIM_MOD	**Universal Interface Mode Select.** Selects the VGA interface mode (see table below).
4	UIM_DCLK	**Universal Interface MUX Control & Data Clock Mode.** Setting this bit inverts the edge at which the input control and data is latched. Refer to Table 5 for details.
5	UIM_CCLK	**Universal Interface MUX Control Clock Mode.** Setting this bit inverts the edge at which the input control is latched. Refer to Table 2.9 for details.
6	Reserved	Reserved (set to 0b).
7	UIM_DEC_EN	**Universal Interface MUX Decimator.** Turns on the horizontal pre-scaler divide by 2 to support 1024 x 720 and above. Refer to the I2C_HDSC/HUSC register at offset 0x0A.
8	UV_SWAP	**Color Swap.** Swaps the Cr and Cb, U and V, or Red and Blue internal input signals in the UIM.
9	UIM_SDFT	**Derive Field Timing Mode.** Specialized timing input mode using HSYNC and VSYNC to also derive field information. When negative edges of HSYNC and VSYNC coincide its field 1 and when they don't its field 2. Works with 13.5 MHz input only. Enables 1:2 UIM bridge, two wire syncs, and encoder input after the 4:4:4 to 4:2:2 conversion.
10	BRDG_SYNC	**Bridge Pointer Reset Down.** Setting this bit enables a pointer reset of the input VGA clock bridge FIFO for seven VSyncs. A low-to-high transition of this bit immediately resets the pointers. **Note:** It's recommended that this bit be set after switching clock settings and after programming the PLL.
11	Reserved	Reserved (set to 0b).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	HUS_DBL_EN	TV_SHORT_FLD	UIM_E	Reserved	BRDG_SYNC	UIM_SDFT	UV_SWAP	UIM_DEC_EN	Reserved	UIM_CCLK	UIM_DCLK	UIM_MOD_3	UIM_MOD_2	UIM_MOD_1	UIM_MOD_0

Bits	Name	Description
12	UIM_E	**UIM Control/Data Eye**. In multiplexed modes, setting this bit combines the previous two words before a control transition into one pixel; otherwise, a pixel contains the word before and after a control transition. It does so by selecting the control signal triggered off of the opposite clock edge as normal. UIM_E must be cleared in non-multiplexed modes. This bit is normally set to 0b.
13	TV_SHORT_FLD	Enables short field mode in the FIFO (and CAC).
14	HUS_DBL_EN	**Horizontal Upscaler Doubling Mode Enable.** Setting this bit to 1b doubles the HUS upscaling value. Refer to the I2C_HDSC/HUSC register at offset 0x0A.
15	Reserved	Reserved (set to 0b),

Table 2.3 GCC RGB Port Mapping Modes

UIM_MOD P Port	0 M888D		1 M888I		1 M565I		2 M555	3 N888	3 N666	3 N565[1]
	MUX Low	MUX High	MUX Low	MUX High	MUX Low	MUX High				
P23	X	X	X	X	X	X	RESERVED	R7	R5	R4
P22	X	X	X	X	X	X		R6	R4	R3
P21	X	X	X	X	X	X		R5	R3	R2
P20	X	X	X	X	X	X		R4	R2	R1
P19	X	X	X	X	X	X		R3	R1	R0
P18	X	X	X	X	X	X		R2	R0	0
P17	X	X	X	X	X	X		R1	0	0
P16	X	X	X	X	X	X		R0	0	0
P15	X	X	X	X	X	X		G7	G5	G5
P14	X	X	X	X	X	X		G6	G4	G4
P13	X	X	X	X	X	X		G5	G3	G3
P12	X	X	X	X	X	X		G4	G2	G2
P11	G3	R7	G4	R7	G2	R4		G3	G1	G1
P10	G2	R6	G3	R6	G1	R3		G2	G0	G0
P9	G1	R5	G2	R5	G0	R2		G1	0	0
P8	G0	R4	B7	R4	B4	R1		G0	0	0
P7	B7	R3	B6	R3	B3	R0		B7	B5	B4
P6	B6	R2	B5	G7	B2	G5		B6	B4	B3
P5	B5	R1	B4	G6	B1	G4		B5	B3	B2
P4	B4	R0	B3	G5	B0	G3		B4	B2	B1
P3	B3	G7	G0	R2	0	0		B3	B1	B0
P2	B2	G6	B2	R1	0	0		B2	B0	0
P1	B1	G5	B1	R0	0	0		B1	0	0
P0	B0	G4	B0	G1	0	0		B0	0	0

1. N656 mode: All unused inputs (input pins) must be grounded in this mode (for example, pins P8, P9, P16, P17, and P18)

Note: *UIM_MOD Mapping: The Universal Input Mux (UIM) UIM_MOD bits select the mode for P23-P0. The intention is to support as many different 3D and GCC graphic controllers, CPU support chips and integrated CPUs as possible (collectively referred to in this datasheet as GCC). lists the mapping in each mode for the digital RGB from the GCC to the appropriate port or extended port pin.*

Table 2.4 GCC YCrCb Port Mapping Modes

UIM_MOD P Port	4 M444C		5 M444T1		6 M565T2		7 M422		8 N656	9 N601	10 N444
	MUX Low	MUX High	MUX Low	MUX High	MUX Low	MUX High	MUX Low	MUX High			
P23	X	X	X	X	X	X	X	X	X	X	Cb7
P22	X	X	X	X	X	X	X	X	X	X	Cb6
P21	X	X	X	X	X	X	X	X	X	X	Cb5
P20	X	X	X	X	X	X	X	X	X	X	Cb4
P19	X	X	X	X	X	X	X	X	X	X	Cb3
P18	X	X	X	X	X	X	X	X	X	X	Cb2
P17	X	X	X	X	X	X	X	X	X	X	Cb1
P16	X	X	X	X	X	X	X	X	X	X	Cb0
P15	X	X	X	X	X	X	X	X	X	C7	Cr7
P14	X	X	X	X	X	X	X	X	X	C6	Cr6
P13	X	X	X	X	X	X	X	X	X	C5	Cr5
P12	X	X	X	X	X	X	X	X	X	C4	Cr4
P11	Cr7	Y7	Y3	Cr7	Y4	Cr7	C7	Y7	YC7	C3	Cr3
P10	Cr6	Y6	Y2	Cr6	Y3	Cr6	C6	Y6	YC6	C2	Cr2
P9	Cr5	Y5	Y1	Cr5	Y2	Cr5	C5	Y5	YC5	C1	Cr1
P8	Cr4	Y4	Y0	Cr4	Cb7	Cr4	C4	Y4	YC4	C0	Cr0
P7	Cr3	Y3	Cb7	Cr3	Cb6	Cr3	C3	Y3	YC3	Y7	Y7
P6	Cr2	Y2	Cb6	Cr2	Cb5	Y7	C2	Y2	YC2	Y6	Y6
P5	Cr1	Y1	Cb5	Cr1	Cb4	Y6	C1	Y1	YC1	Y5	Y5
P4	Cr0	Y0	Cb4	Cr0	Cb3	Y5	C0	Y0	YC0	Y4	Y4
P3	Cb7	Cb3	Cb3	Y7	Y0	Cr2	X	X	X	Y3	Y3
P2	Cb6	Cb2	Cb2	Y6	Cb2	Cr1	X	X	X	Y2	Y2
P1	Cb5	Cb1	Cb1	Y5	Cb1	Cr0	X	X	X	Y1	Y1
P0	Cb4	Cb0	Cb0	Y4	Cb0	Y1	X	X	X	Y0	Y0

Table 2.5 Input Port Clocking

Mode	UIM_CCLK (0x0E)	UIM_DCLK (0x0E)	Control	MUX Low Word	MUX High Word	Notes
Non-MUX[1]	High	High	↓ PCLK	↑PCLK	↑PCLK	
Non-MUX[1]	Low	High	↑PCLK	↑ PCLK	↑ PCLK	See Figure 1 for illustration
Non-MUX[1]	High	Low	↑PCLK	↓ PCLK	↓ PCLK	
Non-MUX[1]	Low	Low	↓ PCLK	↓ PCLK	↓ PCLK	
MUX[2]	High	High	↓ PCLK	↑ PCLK	↓ PCLK	
MUX[2]	Low	High	↑PCLK	↑PCLK	↓ PCLK	
MUX[2]	High	Low	↑PCLK	↓ PCLK	↑PCLK	
MUX[2]	Low	Low	↓ PCLK	↓ PCLK	↑PCLK	See Figure 2 for illustration

1. Non-MUX modes: UIM_MOD 3, 8, 9, 10
2. MUX modes: UIM_MOD 0, 1, 2, 4, 5, 6, 7

Figure 1 Non- MUX Mode Timing Example

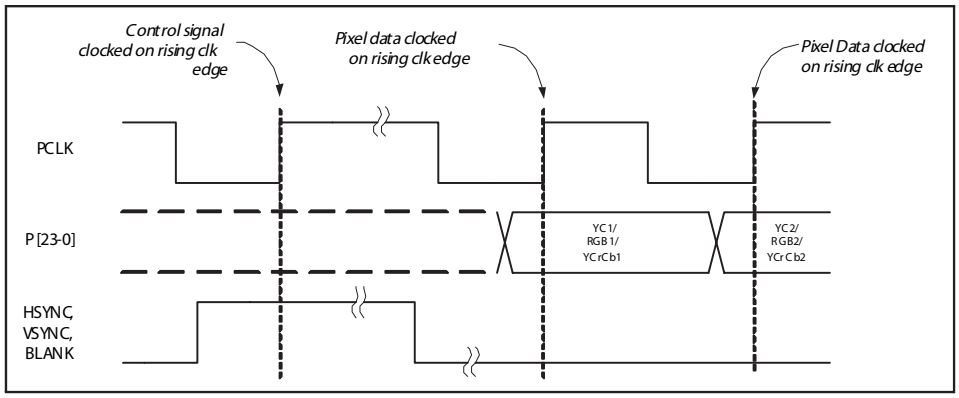
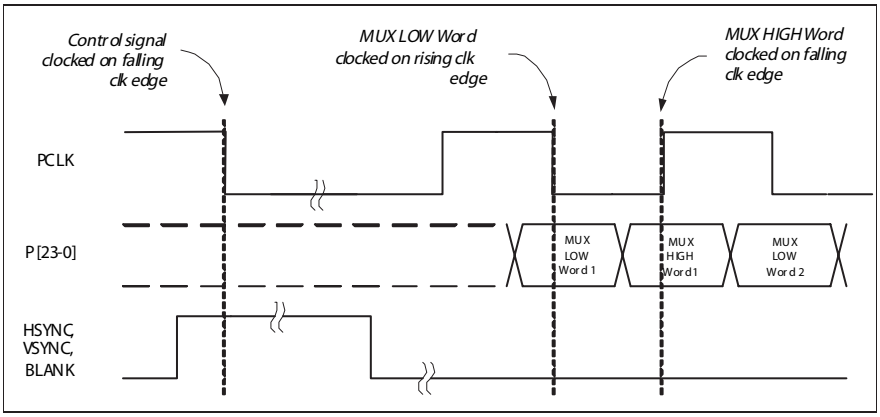


Figure 2 MUX Mode Timing Example



2.2.9 I2C_MISC - Miscellaneous Bits Register 2 (0x10)

- Address Offset - 0x10
- Default Value - 0x000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$GCC\_DRV\_SEL_3$	$P656\_DRV\_SEL_2$	$SYNC\_DRV\_SEL_1$	$SDA\_DRV\_SEL_0$

Bits	Name	Description
0	SDA_DRV_SEL	Set for output drive strength for SDA to be 12ma. Clear for 4Ma
1	SYNC_DRV_SEL	Set for output drive strength for HSYNC, VSYNC, and FIELD to be 12ma. Clear for 4mA
2	P656_DRV_SEL	Set for output drive strength for GPIO0-8 and PBLANK to be 12ma. Clear for 4mA
3	GCC_DRV_SEL	Set for output drive strength for GCC clock to be 12ma. Clear for 4mA
7:4	Not Accessible	Not accessible (set to 0x0).
15:8	Reserved	Reserved (set to 0x0).

2.2.10 I2C_RTCNL - Numerator of Rate Converter Word Low (0x12)

- Address Offset - 0x12
- Default Value - 0x2B7D
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0x00_0000:0xFF_FFFF} RTCN >= RTCD > 0 - where RTCN/RTCD is the ratio of TV clock to a 27 MHz clock

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$RTCN_{15}$	$RTCN_{14}$	$RTCN_{13}$	$RTCN_{12}$	$RTCN_{11}$	$RTCN_{10}$	$RTCN_{9}$	$RTCN_{8}$	$RTCN_{7}$	$RTCN_{6}$	$RTCN_{5}$	$RTCN_{4}$	$RTCN_{3}$	$RTCN_{2}$	$RTCN_{1}$	$RTCN_{0}$

Bits	Name	Description
15:0	RTCN	**Numerator of Rate Converter Word [23:0].** Numerator of fraction used in the rate converter. RTCN is a 24-bit unsigned number.

2.2.11 I2C_RTCNH - Numerator of Rate Converter Word High (0x14)

- Address Offset - 0x14
- Default Value - 0x0048
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0x00_0000:0xFF_FFFF} RTCN >= RTCD > 0 - where RTCN/RTCD is the ratio of TV clock to a 27 MHz clock

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$RTCN_{23}$	$RTCN_{22}$	$RTCN_{21}$	$RTCN_{20}$	$RTCN_{19}$	$RTCN_{18}$	$RTCN_{17}$	$RTCN_{16}$

Bits	Name	Description
7:0	RTCN[23:18]	**Numerator of Rate Converter Word [23:0].** Numerator of fraction used in the rate converter. RTCN is a 24-bit unsigned number.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.12 I2C_RTCDL - Denominator of Rate Converter Word Low (0x16)

- Address Offset - 0x16
- Default Value - 0x2B7D
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0x00_0000:0xFF_FFFF} RTCN >= RTCD > 0 - where RTCN/RTCD is the ratio of TV clock to a 27 MHz clock

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$RTCD_{15}$	$RTCD_{14}$	$RTCD_{13}$	$RTCD_{12}$	$RTCD_{11}$	$RTCD_{10}$	$RTCD_9$	$RTCD_8$	$RTCD_7$	$RTCD_6$	$RTCD_5$	$RTCD_4$	$RTCD_3$	$RTCD_2$	$RTCD_1$	$RTCD_0$

Bits	Name	Description
15:0	RTCD	**Denominator of Rate Converter Word [23:0].** Denominator of fraction used in the rate converter. RTCD is a 24-bit unsigned number.

2.2.13 I2C_RTCDH - Denominator of Rate Converter Word High (0x18)

- Address Offset - 0x18
- Default Value - 0x0048
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0x00_0000:0xFF_FFFF} RTCN >= RTCD > 0 - where RTCN/RTCD is the ratio of TV clock to a 27 MHz clock

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$RTCD_{23}$	$RTCD_{22}$	$RTCD_{21}$	$RTCD_{20}$	$RTCD_{19}$	$RTCD_{18}$	$RTCD_{17}$	$RTCD_{16}$

Bits	Name	Description
7:0	RTCD[23:18]	**Numerator of Rate Converter Word [23:0].** Numerator of fraction used in the rate converter. RTCN is a 24-bit unsigned number.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.14 I2C_HWIDTH - Horizontal Width (0x1A)

- Address Offset - 0x1A
- Default Value - 858d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$HWMIDTH_{10}$	$HWMIDTH_9$	$HWMIDTH_8$	$HWMIDTH_7$	$HWMIDTH_6$	$HWMIDTH_5$	$HWMIDTH_4$	$HWMIDTH_3$	$HWMIDTH_2$	$HWMIDTH_1$	$HWMIDTH_0$

Bits	Name	Description
10:0	HWIDTH	**Horizontal Width [10:0].** Used only for master mode when the FS471 is providing video control signals to the GCC. Set HWIDTH to the total number of horizontal pixels (minus 1) of the GCC video. HWIDTH = (HTOTAL - 1) If HTOTAL is greater than 1024, device must use decimation mode, in which case HWIDTH = (HTOTAL/2 -1). Zero based.
15:11	Not Accessible	Not accessible (set to 0x0).

2.2.15 I2C_HSYNCS - Horizontal Sync Start (0x1C)

- Address Offset - 0x1C
- Default Value - 74d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$HSYNCS_{10}$	$HSYNCS_9$	$HSYNCS_8$	$HSYNCS_7$	$HSYNCS_6$	$HSYNCS_5$	$HSYNCS_{S4}$	$HSYNCS_3$	$HSYNCS_2$	$HSYNCS_1$	$HSYNCS_0$

Bits	Name	Description
10:0	HSYNCS	**Horizontal Sync Start [10:0**]. Used only for master mode when the FS471 is providing video control signals to the GCC. This value represents the GCC input horizontal sync start location in pixels prior to the start of active video (minus 1). HSYNCS = (# of pixels - 1). If HTOTAL is greater than 1024 and the device is in decimation mode, HSYNCS = (# of pixels / 2) -1). Zero based.
15:11	Not Accessible	Not accessible (set to 0x0).

2.2.16 I2C_HSYNCE - Horizontal Sync End (0x1E)

- Address Offset - 0x1E
- Default Value - 138d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$HSYNCE_{10}$	$HSYNCE_9$	$HSYNCE_8$	$HSYNCE_7$	$HSYNCE_6$	$HSYNCE_5$	$HSYNCE_4$	$HSYNCE_3$	$HSYNCE_2$	$HSYNCE_1$	$HSYNCE_0$

Bits	Name	Description
10:0	HSYNCE	**Horizontal Sync End [10:0].** Used only for master mode when the FS471 is providing video control signals to the GCC. This value represents the GCC input horizontal sync end location in pixels prior to the start of active video (minus 1). HSYNCE = (# of pixels - 1). If HTOTAL is greater than 1024 and the device is in decimation mode, HSYNCE = (# of pixels / 2) -1). Zero based.
15:11	Not Accessible	Not accessible (set to 0x0).

2.2.17 I2C_SHP - Flicker Filter Sharpness (0x20)

- Address Offset - 0x20
- Default Value - 0d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:31} Provides 0 to 31/16 (aprox. 6 dB) joint horizontal and vertical high frequency boost

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	SHP_4	SHP_3	SHP_2	SHP_1	SHP_0

Bits	Name	Description
4:0	SHP	**Flicker Filter Sharpness [4-0].** SHP accentuates the joint high vertical/high horizontal frequencies to sharpen edges. SHP is an unsigned number. **Note:** The flicker filter and sharpness filter are not implemented or necessary for vertical scaling factors of two or greater.
15:5	Not Accessible	Not accessible (set to 0x0).

2.2.18 I2C_FLK - Flicker Filter Coefficient (0x22)

- Address Offset - 0x22
- Default Value - 12d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: 16} Provides 0 to 16/16 coefficient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	FLK_4	FLK_3	FLK_2	FLK_1	FLK_0

Bits	Name	Description
4:0	FLK	**Flicker Filter Coefficient [4:0].** Provides a weighting factor for flicker filter. FLK is an unsigned number. **Note:** The flicker filter and sharpness filter are not implemented or necessary for vertical scaling factors of two or greater.
15:5	Not Accessible	Not accessible (set to 0x0).

2.2.19 I2C_GPIO - General Purpose Input Outputs (0x24)

- Address Offset - 0x24
- Default Value - 0000000XXXXXXXXXb
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$GPIO\_OE_{15}$	$GPIO\_OE_{14}$	$GPIO\_OE_{13}$	$GPIO\_OE_{12}$	$GPIO\_OE_{11}$	$GPIO\_OE_{10}$	$GPIO_9$	$GPIO_8$	$GPIO_7$	$GPIO_6$	$GPIO_5$	$GPIO_4$	$GPIO_3$	$GPIO_2$	$GPIO_1$	$GPIO_0$

Bits	Name	Description
4:0	GPIO[8:0]	**General Purpose I/O.** Register writes to and reads from GPIO pins. If corresponding OE controls are set, GPIO reads contain the same data as previously written. If OE controls are cleared, GPIO reads copy the external pin input values.
15:9	GPIO_OE[6:0]	**General Purpose Output Enable.** Enables GPIO register contents to the corresponding pin outputs. GPIO_OE6 enables GPIO8:6.

2.2.20 (0x26) Reserved

2.2.21 (0x28) Reserved

2.2.22 (0x2A) Reserved

2.2.23 (0x2C) Reserved

2.2.24 I2C_PART - Part Identification Number (0x2E)

- Address Offset - 0x2E
- Default Value - 0xFE07
- Attribute - R
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_{15}	ID_{14}	ID_{13}	ID_{12}	ID_{11}	ID_{10}	ID_9	ID_8	ID_7	ID_6	ID_5	ID_4	ID_3	ID_2	ID_1	ID_0

Bits	Name	Description
15:0	ID	**Part Number [15:0].** Identifies the part identification number for software ID purposes.

2.2.25 I2C_SP - Status Port (0x30)

- Address Offset - 0x30
- Default Value - N/A
- Attribute - R
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FIFO_ST	CACQ_ST

Bits	Name	Description
0	CACQ_ST	**Counter Acquire Status.** Status of TV Counter Acquisition (equals 1b if re-acquired). Refer to the CR register to clear.
1	FIFO_ST	**FIFO Status.** Output FIFO status (equals 1b if over/under flowed). Refer to the CR register to clear.
7:2	Reserved	Reserved (set to 0x0).
14:8	Not Accessible	Not accessible (set to 0x0).
15	Reserved	Reserved (set to 0x0).

2.2.26 I2C_FFO - FIFO Status Port (0x32)

- Address Offset - 0x32
- Default Value - N/A
- Attribute - R
- Size - 16 bits
- Allowed Range - {0: 255}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$FFOH_7$	$FFOH_6$	$FFOH_5$	$FFOH_4$	$FFOH_3$	$FFOH_2$	$FFOH_1$	$FFOH_0$	$FFOL_7$	$FFOL_6$	$FFOL_5$	$FFOL_4$	$FFOL_3$	$FFOL_2$	$FFOL_1$	$FFOL_0$

Bits	Name	Description
7:0	FFOL[7:0]	**FIFO Status Port Full [7:0].** This register indicates half the peak excursion of FIFO memory write address minus read address (multiply by eight to get the number of pixels). Relevant to over-run. Unsigned number. Refer to the CR register to clear.
15:8	FFOH[7:0]	**FIFO Status Port Empty [7:0].** This register indicates half the peak excursion of FIFO memory read address minus write address (multiply by eight to get the number of pixels). Relevant to under-run. Unsigned number. Refer to the CR register to clear.

Note: *FIFO Status: FS471 does not have a frame memory, so the scaled input data rate and the output data rates are the same. The FIFO compensates during the asynchronous horizontal blanking interval of the input and output.*

If a data over-run occurs, the FIFO data over-run flag is set.

2.2.27 I2C_FFO_LAT - FIFO Latency (0x34)

- Address Offset - 0x34
- Default Value - 130d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: 511}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	FFO_LAT_8	FFO_LAT_7	FFO_LAT_6	FFO_LAT_5	FFO_LAT_4	FFO_LAT_3	FFO_LAT_2	FFO_LAT_1	FFO_LAT_0

Bits	Name	Description
8:0	FFO_LAT	**FIFO Latency [8:0].** Multiple of output clock cycles between the initiation of VGA writes to the FIFO memory and the TV reads from it. Multiply by eight to get the number of 27 MHz TV clock delays, or by four to get the number of 13.5 MHz TV pixel delays.
15:9	Not Accessible	Not accessible (set to 0x0).

Table 2.1 FIFO Latency

VSC Range	FFO_LAT
0.5 to 1	0x60 (96d)
1 to 2	0x140 (320d)
2 to 4	0x1A0 (416d)

Note: *The values in Table 2.1 are recommendations that should be acceptable in the majority of cases. It's recommended to set and clear bit 6 of (0x0C) and then read bit 1 of 0x30 to verify that there is no overflow condition.*

2.2.28 I2C_VWIDTH - Vertical Width (0x36)

- Address Offset - 0x36
- Default Value - 525d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: 1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$VWDTH_{10}$	$VWDTH_9$	$VWDTH_8$	$VWDTH_7$	$VWDTH_6$	$VWDTH_5$	$VWDTH_4$	$VWDTH_3$	$VWDTH_2$	$VWDTH_1$	$VWDTH_0$

Bits	Name	Description
10:0	VWDTH	**Vertical Width [10:0].** Used only for master mode when the FS471 is providing video control signals to the GCC. Set VWIDTH to the total number of vertical lines (minus 1) of the GCC video: VWIDTH = (VTOTAL - 1). If VTOTAL is greater than 1024, then the device must use decimation mode, in which case VWIDTH = (VTOTAL/2 -1). Zero based.
15:11	Not Accessible	Not accessible (set to 0x0).

2.2.29 I2C_VSYNCS - Vertical Sync Start (0x38)

- Address Offset - 0x38
- Default Value - 42d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: 1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$VSYNCS_{10}$	$VSYNCS_9$	$VSYNCS_8$	$VSYNCS_7$	$VSYNCS_6$	$VSYNCS_5$	$VSYNCS_4$	$VSYNCS_3$	$VSYNCS_2$	$VSYNCS_1$	$VSYNCS_0$

Bits	Name	Description
10:0	VSYNCS	**Vertical Width [10:0].** Used only for master mode when the FS471 is providing video control signals to the GCC. Set VWIDTH to the total number of vertical lines (minus 1) of the GCC video: VWIDTH = (VTOTAL - 1). If VTOTAL is greater than 1024, then the device must use decimation mode, in which case VWIDTH = (VTOTAL/2 -1). Zero based.
15:11	Not Accessible	Not accessible (set to 0x0).

2.2.30 I2C_VSYNCE - Vertical Sync End (0x3A)

- Address Offset - 0x3A
- Default Value - 45d
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0: 1024}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$VSYNCE_{10}$	$VSYNCE_9$	$VSYNCE_8$	$VSYNCE_7$	$VSYNCE_6$	$VSYNCE_5$	$VSYNCE_4$	$VSYNCE_3$	$VSYNCE_2$	$VSYNCE_1$	$VSYNCE_0$

Bits	Name	Description
10:0	VSYNCE	**Vertical Sync End [10:0].** Used only for master mode when the FS471 is providing video control signals to the GCC. This value represents GCC input vertical sync end location in lines prior to the start of active video (minus 1). VSYNCE = (# of Lines -1). If VTOTAL is greater than 1024 and the device is in decimation mode, VSYNCE = [(# of Lines/ 2) -1]. Zero based.
15:11	Not Accessible	Not accessible (set to 0x0).

2.2.31 I2C_VID_CNTL0 - Video Control 0 (0x3C)

- Address Offset - 0x3C
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	OBIN_USIG	Not Accessible	Not Accessible	BLANK_INV	FIELD_INV	VSYNC_INV	HSYNC_INV	INT_PROG	FIELD_MS	Not Accessible	Not Accessible	Not Accessible	MATRIX_BYP	Not Accessible	VID_MODE

Bits	Name	Description
0	VID_MODE	**Video Output Mode.** Refer to Table 2.6.
1	Not Accessible	Not accessible (set to 0x0).
2	MATRIX_BYP	**Matrix Bypass.** When set, bypasses the RGB to YUV matrix. Refer to Table 2.6.
5:3	Not Accessible	Not accessible (set to 0x0).
6	FIELD_MS	**Field Master or Slave.** Set to 1b to enable the field output (master mode only). When cleared, the incoming field is determined by the incoming HSYNC and VSYNC phase relationship.
7	INT_PROG	Set to 1b to enable the field output (master mode only).
8	HSYNC_INV	**Horizontal Sync Invert.** When set, inverts the polarity of the incoming HSync.
9	VSYNC_INV	**Vertical Sync Invert.** When set, inverts the polarity of the incoming VSync.
10	FIELD_INV	**Field Invert.** When set, inverts the polarity of the incoming field. **Note:** Dependency with register 0x3E.
11	BLANK_INV	**Blank Invert.** When set, inverts the polarity of the incoming blank.
13:12	Not Accessible	Not accessible (set to 0x0).
14	OBIN_USIG	**Offset Binary or Unsigned.** When set, RED_SCL, GRN_SCL, and BLU_SCL process input data in the YCrCb offset binary format. If clear, input data is scaled in the RGB unsigned format. Refer to Table 2.6.
15	Not Accessible	Not accessible (set to 0x0).

Table 2.6 Video Output Modes

Video Output Mode	VID_MODE	DAC_AMUX	DAC_BMUX	Encoder Mode	DAC A	DAC B
Composite	0	0	0	Normal	CVBS	GND
Composite	0	0	1	Normal	CVBS	CVBS
Composite	0	1	0	Normal	GND	GND
Composite	0	1	1	Normal	GND	CVBS
S-Video	1	0	0	Normal	Y	C
S-Video	1	0	1	Normal	Y	Y
S-Video	1	1	0	Normal	C	C
S-Video	1	1	1	Normal	C	Y

2.2.32 I2C_FLD_DLY - Field Delay Value (0x3E)

- Address Offset - 0x3E
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD_DLY_INV	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$FIELD\_DLY_{10}$	$FIELD\_DLY_{9}$	$FIELD\_DLY_{8}$	$FIELD\_DLY_{7}$	$FIELD\_DLY_{6}$	$FIELD\_DLY_{5}$	$FIELD\_DLY_{4}$	$FIELD\_DLY_{3}$	$FIELD\_DLY_{2}$	$FIELD\_DLY_{1}$	$FIELD\_DLY_{0}$

Bits	Name	Description
10:0	FIELD_DLY[10:0]	**Field Delay Value.** Used only for master mode when the FS471 is providing video control signals to the GCC. Delays the transition of the field output from the timing generator, by this value in input lines. **Note:** If set to zero, the video field invert control (bit 10 in register 0x3C) is enabled for this output and the field delay output functionality becomes FIELD_DLY_INV XOR FIELD_INV.
11:14	Not Accessible	Not accessible (set to 0x0).
15	FIELD_DLY_INV	**Field Delay Invert.** Delays the transition of the field output by an entire field by inverting it. Refer to the FIELD_DLY[10:0] note.

2.2.33 ENC_CHR_FREQ0 - Chroma Sub-Carrier Frequency Low (0x40)

- Address Offset - 0x40
- Default Value - 0x7C1F
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHR_FREQ_{15}	CHR_FREQ_{14}	CHR_FREQ_{13}	CHR_FREQ_{12}	CHR_FREQ_{11}	CHR_FREQ_{10}	CHR_FREQ_{9}	CHR_FREQ_{8}	CHR_FREQ_{7}	CHR_FREQ_{6}	CHR_FREQ_{5}	CHR_FREQ_{4}	CHR_FREQ_{3}	CHR_FREQ_{2}	CHR_FREQ_{1}	CHR_FREQ_{0}

Bits	Name	Description
15:0	CHR_FREQ	**Chroma Sub-Carrier Frequency.** Sets the sub-carrier frequency according to the equation shown in the note that follows. Refer to Table 2-8 for suggested register values and the bit order (15:0).

Note:

$$CHR\_FREQ = \left(\frac{Subcarrier}{27\ MHz} \right) * 2^{32}$$

Where:

NTSC Subcarrier = 3.57954545

PAL Subcarrier = 4.43361875

2.2.34 ENC_CHR_FREQ2 - Chroma Sub-Carrier Frequency High (0x42)

- Address Offset - 0x42
- Default Value - 0x21F0
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHR_FREQ_{31}	CHR_FREQ_{30}	CHR_FREQ_{29}	CHR_FREQ_{28}	CHR_FREQ_{27}	CHR_FREQ_{26}	CHR_FREQ_{25}	CHR_FREQ_{24}	CHR_FREQ_{23}	CHR_FREQ_{22}	CHR_FREQ_{21}	CHR_FREQ_{20}	CHR_FREQ_{19}	CHR_FREQ_{18}	CHR_FREQ_{17}	CHR_FREQ_{16}

Bits	Name	Description
15:0	CHR_FREQ	**Chroma Sub-Carrier Frequency.** Sets the sub-carrier frequency according to the equation shown in the note under paragraph 2.2.33. Refer to Table 2-8 for suggested register values and the bit order (31:15).

2.2.35 ENC_CHR_PHASE - Chroma Phase (0x44)

- Address Offset - 0x44
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	CHR_PHASE_{7}	CHR_PHASE_{6}	CHR_PHASE_{5}	CHR_PHASE_{4}	CHR_PHASE_{3}	CHR_PHASE_{2}	CHR_PHASE_{1}	CHR_PHASE_{0}

Bits	Name	Description
15:0	CHR_PHASE	**Pre-Set Sub-Carrier Phase [7:0].** Value for pre-set sub-carrier phase (only the upper 8 bits are programmable. The lower 24 bits equal 0x0). The angle is CHR_PHASE/256*360 and is normally zero.

2.2.36 ENC_MISC - Encoder Miscellaneous Registers 0 and 1 (0x46)

- Address Offset - 0x46
- Default Value - 0x0900
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	YC_DELAY_2	YC_DELAY_1	YC_DELAY_0	CVBS_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CLRBAR	BYPCLP

Bits	Name	Description
0	BYPCLP	**Bypass Y Clamp.** Allows for non-standard range of luma on Y-inputs. 0b = the luma expected range [16:235], and clamped to this range. 1b = luma is expected in range [0:255] and no clamping is performed.
1	CLRBAR	**Color Bar Mode.** Causes the YC inputs in the encoder to be ignored and forces a color bar pattern onto the input. The color bar pattern is a repeating sequence of eight colors at 75% amplitude and 100% saturation. The color bars are based on input HSYNC and VSYNC if these signals are present. If HSYNC and VSYNC signals are not provided, the color bar generator creates its own SYNC reference.
7:2	Reserved	Reserved (set to 0x0).
8	CVBS_EN	**CVBS Enable.** Enables composite and luma outputs. No need to change for the FS471. (1b = CVBS enabled).
11:9	YC_DELAY[2:0]	**YC Delay.** Relative pipeline delay between luma and chroma outputs (4=0 clock; 0=luma lags chroma by 4 clocks; 7=chroma lags luma by 3 clocks).
15:12	Reserved	Reserved (set to 0x0).

2.2.37 ENC_RGB_YUV - Chroma Gain and Bandwidth Control (0x48)

- Address Offset - 0x48
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Reserved	Reserved	Reserved	Reserved	CHR_BW_1	Reserved	$COMP\_GAIN_1$	$COMP\_GAIN_0$

Bits	Name	Description
1:0	COMP_GAIN[1:0]	**Composite Chroma Gain.** Percentage of chroma used in composite output. 00b = 100% 01b = 25% 10b = 50% 11b = 75%
2	Reserved	Reserved
3	CHR_BW[1]	**Chroma Filter Bandwidth Control.** 00b = Composite 01b = Wide (NTSC S-Video) 10b = Extra wide (PAL S-Video) **Note:** One of two bits controlling chroma. For bit 0, refer to register 0x7E (ENC_UV_STUFF).
7:4	Reserved	Reserved
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.38 ENC_HSYNC_W - Horizontal Sync Width (0x4A)

- Address Offset - 0x4A
- Default Value - 0xXX7Eh
- Attribute - R/W
- Size - 16 bits
- Allowed Range - 16d < ENC_HSYNC_W < (active line + front porch + back porch)}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$HSYNC\_WID_7$	$HSYNC\_WID_6$	$HSYNC\_WID_5$	$HSYNC\_WID_4$	$HSYNC\_WID_3$	$HSYNC\_WID_2$	$HSYNC\_WID_1$	Not Accessible

Bits	Name	Description
0	Not Accessible	Not accessible.
2	HSYNC_WID[7:1]	**HSync Width.** Width of HSync in 27 MHz clocks (LSB bit 0 is tied to zero).
15:8	Not Accessible	Not accessible.

2.2.39 ENC_BRST_W - Burst Width (0x4C)

- Address Offset - 0x4C
- Default Value - 0xXX44 (68d)
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:127}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Reserved	$BURST\_WID_6$	$BURST\_WID_5$	$BURST\_WID_4$	$BURST\_WID_3$	$BURST\_WID_2$	$BURST\_WID_1$	$BURST\_WID_0$

Bits	Name	Description
6:0	BURST_WID[6:0]	**Burst Width.** Width of the SDTV color burst in 27 MHz clocks. **Note:** HSYNC_WID plus BURST_WID must be a multiple of four clocks and less than ¾ total line width.
7	Reserved	Reserved.
15:8	Not Accessible	Not accessible.

2.2.40 ENC_BP_LOC - Back Porch Width (0x4E)

- Address Offset - 0x4E
- Default Value - 0xXX76
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:256}, burst width + breezeway + 16d < BP_LOC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$BPORCH_7$	$BPORCH_6$	$BPORCH_5$	$BPORCH_4$	$BPORCH_3$	$BPORCH_2$	$BPORCH_1$	Reserved

Bits	Name	Description
0	Reserved	Reserved.
7:1	BPORCH[7:1]	**Burst Width.** Width of the SDTV color burst in 27 MHz clocks. **Note:** HSYNC_WID plus BURST_WID must be a multiple of four clocks and less than ¾ total line width.
15:8	Not Accessible	Not accessible.

2.2.41 ENC_CB_B_LVL - Cb Burst Amplitude, Cr Burst Amplitude (0x50)

- Address Offset - 0x50
- Default Value - 0x003B
- Attribute - R/W
- Size - 16 bits
- Allowed Range - 8 bit two's complement {-128:127}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR_BURST_7	CR_BURST_6	CR_BURST_5	CR_BURST_4	CR_BURST_3	CR_BURST_2	CR_BURST_1	CR_BURST_0	CB_BURST_7	CB_BURST_6	CB_BURST_5	CB_BURST_4	CB_BURST_3	CB_BURST_2	CB_BURST_1	CB_BURST_0

Bits	Name	Description
7:0	CB_BURST[7:0]	**Cb Burst Amplitude Setting.** Range {-127:127} normally positive.
15:8	CR_BURST[7:0]	**Cr Burst Amplitude Setting.** Range {-127:127} normally positive.

2.2.42 ENC_SLV_CNTL - Encoder Slave Control (0x52)

- Address Offset - 0x52
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SLV_THRS	SLV_MOD

Bits	Name	Description
0	SLV_MOD	**Slave Mode.** Enable bit for full slave mode timing. Note that this bit is typically set to one. This does not enable partial slave mode and should be cleared unless full slave mode operation is required.
1	SLV_THRS	**Slave Mode Threshold.** Controls the threshold at which the encoder begins the horizontal line adjustments (0=0 line, 1=30 line).
7:2	Reserved	Reserved.
15:8	Not Accessible	Not accessible.

2.2.43 ENC_BLACK_LVLL - Black Level (0x54)

- Address Offset - 0x54
- Default Value - 0x4602
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:1023}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$BLACK\_LVL_9$	$BLACK\_LVL_8$	$BLACK\_LVL_7$	$BLACK\_LVL_6$	$BLACK\_LVL_5$	$BLACK\_LVL_4$	$BLACK\_LVL_3$	$BLACK\_LVL_2$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$BLACK\_LVL_1$	$BLACK\_LVL_0$

Bits	Name	Description
1:0	BLACK_LVL[1:0]	**Black Level.** Used to create the SDTV setup value. *Value must be greater than ENC_BLANK_LVLL.*
7:2	Reserved	Reserved.
15:8	BLACK_LVL[9:2]	**Black Level.** Used to create the SDTV setup value. *Value must be greater than ENC_BLANK_LVLL.*

2.2.44 ENC_BLANK_LVLL - Blank Level (0x56)

- Address Offset: - 0x56
- Default Value: - 0x3C00
- Attribute: - R/W
- Size: - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$BLANK\_LVL_9$	$BLANK\_LVL_8$	$BLANK\_LVL_7$	$BLANK\_LVL_6$	$BLANK\_LVL_5$	$BLANK\_LVL_4$	$BLANK\_LVL_3$	$BLANK\_LVL_2$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$BLANK\_LVL_1$	$BLANK\_LVL_0$

Bits	Name	Description
1:0	BLANK_LVL[1:0]	**Blank Level.** Used to create the SDTV setup value during non-VBI.
7:2	Reserved	Reserved.
15:8	BLANK_LVL[9:2]	**Blank Level.** Used to create the SDTV setup value during non-VBI.

2.2.45 (0x58) Reserved

2.2.46 (0x5A) Reserved

2.2.47 (0x5C) Reserved

2.2.48 ENC_NUM_LINEL - Number of Lines (0x5E)

- Address Offset - 0x5E
- Default Value - 0x8301
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NUM_LINES_9	NUM_LINES_8	NUM_LINES_7	NUM_LINES_6	NUM_LINES_5	NUM_LINES_4	NUM_LINES_3	NUM_LINES_2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NUM_LINES_1	NUM_LINES_0

Bits	Name	Description
1:0	NUM_LINES[1:0]	**Number of Lines.** Number of lines in a frame. Set to 525 for NTSC mode and 625 for PAL mode. **Notes:** 1. NUM_LINES modulo 4 must equal 1. 2. For VSYNC5 = 0: a. If 1ST_LINE >20d, NUM_LINES must be greater than 2*(1ST_LINE + 18d). b. If 1ST_LINE <20d, NUM_LINES must be greater than or equal to 77d. 3. For VYSNC5 = 1: a. If 1STt_LINE >22d, NUM_LINES must be greater than 2*(1st_LINE + 18d). b. If 1ST_LINE < 22d, NUM_LINES must be greater than or equal to 81. • VSYNC5 – Refer to register 0x7E for details. • 1ST_LINE – Refer to register 0x7A for details.
7:2	Reserved	Reserved.
15:8	NUM_LINES[9:2]	**Number of Lines.** Number of lines in a frame. Note that an odd number implies an interlaced image and an even number implies a progressive image. **Notes**: 1. NUM_LINES modulo 4 must equal 1. 2. For VSYNC5 = 0: a. If 1ST_LINE >20d, NUM_LINES must be greater than 2*(1ST_LINE + 18d). b. If 1ST_LINE <20d, NUM_LINES must be greater than or equal to 77d. 3. For VYSNC5 = 1: a. If 1STt_LINE >22d, NUM_LINES must be greater than 2*(1st_LINE + 18d). b. If 1ST_LINE < 22d, NUM_LINES must be greater than or equal to 81. • VSYNC5 – Refer to register 0x7E for details. • 1ST_LINE – Refer to register 0x7A for details

2.2.49 (0x60) Reserved

2.2.50 (0x62) Reserved

2.2.51 ENC_WHITE_LVLL - White Level (0x64)

- Address Offset - 0x64
- Default Value - 0xC800
- Attribute - R/W
- Size - 16 bits
- Allowed Range - {0:1023}, Must be greater than ENC_BLACK_LVLL(54) and ENC_BLANK_LVLL(56)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$WHITE\_LVL_9$	$WHITE\_LVL_8$	$WHITE\_LVL_7$	$WHITE\_LVL_6$	$WHITE\_LVL_5$	$WHITE\_LVL_4$	$WHITE\_LVL_3$	$WHITE\_LVL_2$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$WHITE\_LVL_1$	$WHITE\_LVL_0$

Bits	Name	Description
1:0	WHITE_LVL[1:0]	**White Level.** SDTV white level amplitude.
7:2	Reserved	Reserved.
15:8	WHITE_LVL[9:2]	**White Level.** SDTV white level amplitude.

2.2.52 ENC_CB_GAIN - Cb, Cr Color Saturation (0x66)

- Address Offset - 0x66
- Default Value - 0x8989
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR_GAIN_7	CR_GAIN_6	CR_GAIN_5	CR_GAIN_4	CR_GAIN_3	CR_GAIN_2	CR_GAIN_1	CR_GAIN_0	CB_GAIN_7	CB_GAIN_6	CB_GAIN_5	CB_GAIN_4	CB_GAIN_3	CB_GAIN_2	CB_GAIN_1	CB_GAIN_0

Bits	Name	Description
7:0	CB_GAIN[7:0]	**Cb Color Saturation Control.** (1 LSB = 1/128). **Note:** Varying relative gains between CB and CR can modify Tint.
15:8	CR_GAIN[7:0]	**Cr Color Saturation Control.** (1 LSB = 1/128). **Note:** Varying relative gains between CB and CR can modify Tint.

2.2.53 (0x68) Reserved

2.2.54 ENC_TINT - Tint (0x6A)

- Address Offset - 0x6A
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$TINT_7$	$TINT_6$	$TINT_5$	$TINT_4$	$TINT_3$	$TINT_2$	$TINT_1$	$TINT_0$

Bits	Name	Description
7:0	TINT[7:0]	**Tint Adjustment on Chroma.** Also called Hue. Normally 0x0. Modifies tint by adding phase offset to sub-carrier.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.55 (0x6C) Reserved

2.2.56 (0x6E) Reserved

2.2.57 ENC_BRZ_WAY - Width of Breezeway, Front Porch (0x70)

- Address Offset - 0x70
- Default Value - 0x2016
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	FR_PORCH_5	FR_PORCH_4	FR_PORCH_3	FR_PORCH_2	FR_PORCH_1	Reserved	Reserved	Reserved	Reserved	BR_WAY_4	BR_WAY_3	BR_WAY_2	BR_WAY_1	BR_WAY_0

Bits	Name	Description
4:0	BR_WAY[4:0]	**Width of Breezeway.** Width of breezeway in 27 MHz clocks.
6:4	Reserved	Reserved.
8	Reserved	Reserved (set to 0x0).
13:9	FR_PORCH[5:1]	**Front Porch.** Width of front porch in 27 MHz clocks (LSB bit 0 tied to zero). **Note:** 1. FR_PORCH must be > 8d. 2. LSB (Bit 0) is forced to zero. (Default value is 32d but reads as 16d).
15:14	Reserved	Reserved.

2.2.58 (0x72) Reserved

2.2.59 (0x74) Reserved

2.2.60 (0x76) Reserved

2.2.61 ENC_ACT_LINEL - Active Video Line Pixels (0x78)

- Address Offset - 0x78
- Default Value - 0xB400
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACT_LINE_{10}	ACT_LINE_9	ACT_LINE_8	ACT_LINE_7	ACT_LINE_6	ACT_LINE_5	ACT_LINE_4	ACT_LINE_3	Reserved	Reserved	Reserved	Reserved	Reserved	ACT_LINE_2	ACT_LINE_1	ACT_LINE_0

Bits	Name	Description
2:0	ACT_LINE[2:0]	**Active Video Line.** Number of 27 MHz clocks in active video line (1440 setting refers to 720 of luma pixels and 720 chroma (Cb and Cr) pixels; the LSB bits [1:0] are tied to zero).
7:3	Reserved	Reserved.
15:8	ACT_LINE[10:3]	**Active Video Line.** Number of 27 MHz clocks in active video line (1440 setting refers to 720 of luma pixels and 720 chroma (Cb and Cr) pixels; the LSB bits [1:0] are tied to zero).

2.2.62 ENC_VLINE_1 - First Video Line (0x7A)

- Address Offset - 0x7A
- Default Value - 0xXX15
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$1ST\_LINE_7$	$1ST\_LINE_6$	$1ST\_LINE_5$	$1ST\_LINE_4$	$1ST\_LINE_3$	$1ST\_LINE_2$	$1ST\_LINE_1$	$1ST\_LINE_0$

Bits	Name	Description
7:0	1ST_LINE[7:0]	**First Line of Video.** Line number for the first line of video in a field. Setting to N causes lines 0 to (N-1) to be blanked, with line N being the first active video line. **Note:** 〈 *If VSYNC5 = 1, 8d < 1ST_LINE* 〈 *If VSYNC5 = 0, 10d < 1ST_LINE*\ Refer to Register 0x7E for VSYNC5.
15:8	Not Accessible	Not accessible.

2.2.63 ENC_SFT_RST - Encoder Version, Encoder Soft Reset (0x7C)

- Address Offset - 0x7C
- Default Value - 0x2000
- Attribute - [15-8] = R [7-0] = R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENC_VER_7	ENC_VER_6	ENC_VER_5	ENC_VER_4	ENC_VER_3	ENC_VER_2	ENC_VER_1	ENC_VER_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SOFT_RST

Bits	Name	Description
0	SOFT_RST	**Encoder Soft Reset.** Writing to this bit resets timing generator of the video encoder. **Note:** 1b holds reset state. SOFT_RST might be held high during register programming to prevent unexpected results at the video output.
7:2	Reserved	Reserved.
15:8	ENC_VER[7:0]	**Encoder Version Number.** Contains the version of the encoder. These eight bits are read-only.

2.2.64 ENC_UV_STUFF - Miscellaneous (0x7E)

- Address Offset - 0x7E
- Default Value - 0xXX02
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	UV_ORDER	PAL_MODE	CHR_BW_0	INVERT_TOP	SYS625_50	$CPHASE_1$	$CPHASE_0$	VSYNC5

Bits	Name	Description
0	VSYNC5	**VSync Equalization Pulses.** 0b = 6. 1b = 5 VSync equalization and broad pulses.
1	CPHASE[2:1]	**Resetting Period of Carrier Clock.** 0x0 = Every eight fields. 0x1 = Every four fields. 0x2 = Every other line. 0x3 = Once before any chroma burst and then never resets again.
3	SYS625_50	**System Field Format.** 0b = 525 lines and 59.94 fields/sec system. 1b = 625 lines and 50 fields/sec system.
4	INVERT_TOP	**Invert Field ID Polarity.** Inverts the polarity of the encoder's field identification signal. Normally 0b for NTSC and 1b for PAL. **Note:** When INVERT_TOP is low (NTSC), Field = 0b indicating the top field; Field = 1b indicating the bottom field. When INVERT_TOP is high (PAL), Field = 1b indicating the bottom field; Field = 1b indicating the top field.
5	CHR_BW_0	**Chroma Filter Bandwidth Control.** 00b = Composite. 01b = Wide (NTSC S-Video). 10b = Extra wide (PAL S-Video). ***Note:*** *One of two bits controlling Chroma. Refer to RGB_YUV (0x48) for bit 1.*
6	PAL_MODE	**PAL or NTSC Mode.** 0b = NTSC. 1b = PAL.
7	UV_ORDER	**UV Order.** Switches ordering of Cb and Cr inputs. Set to 0b.
15:8	Not Accessible	Not accessible.

2.2.65 ENC_SYNC_LVL - SYNC Level (0x80)

- Address Offset - 0x80
- Default Value - 0xXX48
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$SYNC\_LVL_7$	$SYNC\_LVL_6$	$SYNC\_LVL_5$	$SYNC\_LVL_4$	$SYNC\_LVL_3$	$SYNC\_LVL_2$	$SYNC\_LVL_1$	$SYNC\_LVL_0$

Bits	Name	Description
7:0	SYNC_LVL[7:0]	**Sync Level.** Sync level during non-VBI lines. **Note:** Value must be less than ENC_BLACK_LVLL (0x54) and ENC_BLANK_LVLL (0x56).
15:8	Not Accessible	Not accessible.

2.2.66 (0x82) Reserved

2.2.67 (0x84) Reserved

2.2.68 (0x86) Reserved

2.2.69 ENC_VBIBL_LVL - VBI Blank Level (0x88)

Address Offset - 0x88

Default Value - 0x4A00

Attribute - R/W

Size - 16 bits

Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$VBIBL\_LVL_9$	$VBIBL\_LVL_8$	$VBIBL\_LVL_7$	$VBIBL\_LVL_6$	$VBIBL\_LVL_5$	$VBIBL\_LVL_4$	$VBIBL\_LVL_3$	$VBIBL\_LVL_2$	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	$VBIBL\_LVL_1$	$VBIBL\_LVL_0$

Bits	Name	Description
1:0	VBIBL_LVL[1:0]	**VBI Blanking Level.** Blanking level during VBI lines.
7:2	Not Accessible	Not accessible (set to 0x0).
15:8	VBIBL_LVL[9:2]	**VBI Blanking Level.** Blanking level during VBI lines.

2.2.70 ENC_WSS - Wide Screen Signaling (0x8A)

- Address Offset - 0x8A
- Default Value - 0xXX07
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Reserved	WSSF1_EN	WSSF0_EN	WSS_TYPE	WSS_CLKBY	WSS_EDGE_2	WSS_EDGE_1	WSS_EDGE_0

Bits	Name	Description
2:0	WSS_EDGE[2:0]	**WSS Edge Rate Control.** Edge rates are proportional to the frequency of the WSS clock, but can also be scaled by the WSS_EDGE parameter. Higher numbers indicate faster rise and fall times on the WSS pulses.
3	WSS_CLKBY	**WSS Clock Bypass.** Typically this is set to 1b in NTSC and 0b in PAL. 1b = Causes the chroma clock to be used as the WSS clock. 0b = Forces the local 12-bit WSS clock to be used.
4	WSS_TYPE	**WSS Type.** 1b = PAL, ITU-R BT.1119-2. 0b = NTSC, EIAJ CPR-1204.
5	WSSF0_EN	**WSS Field 0 Enable.** Enables WSS signal in Field 0.
6	WSSF1_EN	**WSS Field 1 Enable.** Enables WSS signal in Field 1.
7	Reserved	Reserved.
15:8	Not Accessible	Not accessible.

2.2.71 ENC_WSS_CLKL - WSS Clock (0x8C)

- Address Offset - 0x8C
- Default Value - 0x2F07
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSS_CLK_{11}	WSS_CLK_{10}	WSS_CLK_{9}	WSS_CLK_{8}	WSS_CLK_{7}	WSS_CLK_{6}	WSS_CLK_{5}	WSS_CLK_{4}	Not Accessible	Not Accessible	Not Accessible	Not Accessible	WSS_CLK_{3}	WSS_CLK_{2}	WSS_CLK_{1}	WSS_CLK_{0}

Bits	Name	Description
3:0	WSS_CLK[3:0]	**WSS Clock Frequency.** Calculated from: WSS clock frequency / encoder clock frequency.
7:4	Not Accessible	Not accessible (set to 0x0).
15:8	WSS_CLK[11:4]	**WSS Clock Frequency.** Calculated from: WSS clock frequency / encoder clock frequency.

Note: *WSS Clock Frequency = (WSS_CLK / 2^{12}) x (27 MHz).*

2.2.72 ENC_WSS_DF1L - WSS Data Field 1 Low (0x8E)

- Address Offset - 0x8E
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSS_DATF1_{11}	WSS_DATF1_{10}	WSS_DATF1_{9}	WSS_DATF1_{8}	WSS_DATF1_{7}	WSS_DATF1_{6}	WSS_DATF1_{5}	WSS_DATF1_{4}	Not Accessible	Not Accessible	Not Accessible	Not Accessible	WSS_DATF1_{3}	WSS_DATF1_{2}	WSS_DATF1_{1}	WSS_DATF1_{0}

Bits	Name	Description
3:0	WSS_DATF1[3:0]	**WSS Data for Field 1.** A waveform only appears when WSSF1_EN = 1.
7:4	Not Accessible	Not accessible (set to 0x0).
15:8	WSS_DATF1[11:4]	**WSS Data for Field 1.** A waveform only appears when WSSF1_EN = 1.

2.2.73 ENC_WSS_DF1H - WSS Data Field 1 High (0x90)

- Address Offset - 0x90
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	WSS_DATF1_{19}	WSS_DATF1_{18}	WSS_DATF1_{17}	WSS_DATF1_{16}	WSS_DATF1_{15}	WSS_DATF1_{14}	WSS_DATF1_{13}	WSS_DATF1_{12}

Bits	Name	Description
7:0	WSS_DATF1[19:12]	**WSS Data for Field 1.** A waveform only appears when WSSF1_EN = 1.
15:8	Not Accessible	Not accessible.

2.2.74 ENC_WSS_DF0L - WSS Data Field 0 Low (0x92)

- Address Offset - 0x92
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSS_DATF0_{11}	WSS_DATF0_{10}	WSS_DATF0_{9}	WSS_DATF0_{8}	WSS_DATF0_{7}	WSS_DATF0_{6}	WSS_DATF0_{5}	WSS_DATF0_{4}	Not Accessible	Not Accessible	Not Accessible	Not Accessible	WSS_DATF0_{3}	WSS_DATF0_{2}	WSS_DATF0_{1}	WSS_DATF0_{0}

Bits	Name	Description
3:0	WSS_DATF0[3:0]	**WSS Data for Field 0.** A waveform only appears when WSSF0_EN = 1.
7:4	Not Accessible	Not accessible (set to 0x0).
15:8	WSS_DATF0[11:4]	**WSS Data for Field 0.** A waveform only appears when WSSF0_EN = 1.

2.2.75 ENC_WSS_DF0H - WSS Data Field 0 High (0x94)

- Address Offset - 0x94
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	WSS_DATF0_{19}	WSS_DATF0_{18}	WSS_DATF0_{17}	WSS_DATF0_{16}	WSS_DATF0_{15}	WSS_DATF0_{14}	WSS_DATF0_{13}	WSS_DATF0_{12}

Bits	Name	Description
7:0	WSS_DATF0[19:12]	**WSS Data for Field 0.** A waveform only appears when WSSF0_EN = 1.
15:8	Not Accessible	Not accessible.

2.2.76 ENC_WSS_LF0 - Field 0 & Field 1 Line Number (0x96)

- Address Offset - 0x96
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - TBD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSS_LNF1_7	WSS_LNF1_6	WSS_LNF1_5	WSS_LNF1_4	WSS_LNF1_3	WSS_LNF1_2	WSS_LNF1_1	WSS_LNF1_0	WSS_LNF0_7	WSS_LNF0_6	WSS_LNF0_5	WSS_LNF0_4	WSS_LNF0_3	WSS_LNF0_2	WSS_LNF0_1	WSS_LNF0_0

Bits	Name	Description
7:0	WSS_LNF0[7:0]	**Field 0 WSS Line.** Line number (relative to the previous VSync) at which the WSS data appears in Field 0.
15:8	WSS_LNF1[7:0]	**Field 1 WSS Line.** Line number (relative to the previous VSync) at which the WSS data appears in Field 1.

2.2.77 ENC_WSS_LVLL - WSS Level (0x98)

- Address Offset - 0x98
- Default Value - 0xFF03
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSS_LVL_9	WSS_LVL_8	WSS_LVL_7	WSS_LVL_6	WSS_LVL_5	WSS_LVL_4	WSS_LVL_3	WSS_LVL_2	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	WSS_LVL_2	WSS_LVL_1	WSS_LVL_0

Bits	Name	Description
2:0	WSS_LVL[2:0]	**WSS High Level.** WSS waveform rises from VBIBL_LVL to WSS_LVL in a zero-to one transition.
7:3	Not Accessible	Not accessible (set to 0x0).
15:8	WSS_LVL[9:2]	**WSS High Level.** WSS waveform rises from VBIBL_LVL to WSS_LVL in a zero-to one transition.

2.2.78 ENC_NOTCH - Notch Parameters (0x9A)

- Address Offset - 0x9A
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Reserved	Reserved	Reserved	NOTCH_EN	NOTCH_WD	$NOTCH\_FRQ_2$	$NOTCH\_FRQ_1$	$NOTCH\_FRQ_0$

Bits	Name	Description
2:0	NOTCH_FRQ[1:0]	**Notch Frequency.** Selects from eight possible frequencies around which the notch is centered (see table below). Typically two for NTSC and five for PAL.
3	NOTCH_WD	**Notch Filter Wide Bandwidth.** 1b = Wide. 0b = Narrow.
4	NOTCH_EN	**Notch Filter Enable.** 1b = On. 0b = Off.
7:5	Reserved	Reserved.
15:8	Not Accessible	Not accessible (set to 0x0).

Table 2.7 NOTCH_FRQ Values

NOTCH_FRQ	Description	Notch Y Value	Notch Y Value
0		1 + 1/8 + 1/16	1.1875
1		1 + 1/8 + 1/64	1.1406
2	BT. 601 NTSC	1 + 1/8 + 1/16 (wide) 1 (narrow)	1.0938 1.0000
3	SQ Pixel NTSC	1 - 1/128	0.9922
4	SQ Pixel PAL	1 - 1/32 - 1/64	0.9531
5	BT. 601 PAL	1 - 1/8 - 1/32 -1/128 (wide) 1 - 1/4 + 1/32 -1/128 (narrow)	0.8359 0.7734
6		1 - 1/8 - 1/16 - 1/32	0.7813
7		1 - 1/4 - 1/32	0.7188

Table 2.8 Typical Register Values for Various Standards

Hex Index	Register	NTSC	PAL	PAL-M	PAL-N	Combination PAL-N
40	chr_freq low	0x7C1F	0x8ACB	0xEFE3	0x8ACB	0x9446
42	chr_freq high	0x21F0	0x2A09	0x21E6	0x2A09	0x21F6
44	chr_phase	0	0	0	0	0
4A	hsync_wid	126	126	126	126	126
4C	burst_wid	68	64	68	64	68
4E	bporch	118	138	118	138	138
50	cr_burst	0	31	29	29	31
50	cb_burst	59	44	41	41	44
54	black_lvl	282	251	282	282	251
56	blank_lvl	240	251	240	240	251
5E	line_frame	525	625	525	625	625
64	white_lvl	800	800	800	800	800
66	cr_gain	137	145	137	137	145
66	cb_gain	137	145	137	137	145
70	frnt_porch	32	24	32	24	24
70	breeze_way	22	26	18	26	26
78	activeline	1440	1440	1440	1440	1440
7E	vsync5	0	1	0	0	1
7E	cphase	2	0	0	0	0
7E	sys625_50	0	1	0	1	1
7E	INVERT_TOP					
7E	CHR_BW					
7E	pal_mode	0	1	1	1	1
80	sync_lvl	16	16	16	16	16
88	VBIBL_LVl	240	251	240	240	251

Note: *Table 10 settings are for a FS471 (non Macrovision device).*

2.2.79 I2C_DAC_LD_VAL - DAC Load Detect Parameters (0x9C)

- Address Offset 0x9C
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	LD_VAL_9	LD_VAL_8	LD_VAL_7	LD_VAL_6	LD_VAL_5	LD_VAL_4	LD_VAL_3	LD_VAL_2	LD_VAL_1	LD_VAL_0

Bits	Name	Description
9:0	LD_VAL[9:0]	**DAC Load Value.** Selects output value to DAC during a load test.
10	DETECT_DAC_A	**DAC A Load Mask.** When written, selects which DAC A for a load test. Returns the load test answer. Returns a 1b if measured load is less than RThresh.
11	DETECT_DAC_B	**DAC B Load Mask.** When written, selects which DAC B for a load test. Returns a 1b if measured load is less than RThresh.
13:12	Not Accessible	Not accessible (set to 0x0).
14	DETECT_RDY	**Initiate DAC Load Detect.** Set to 1b to initiate a DAC load detection cycle. Returns 1b when the DAC load detection cycle completes. **Note:** Writing a 0b to this bit returns invalid data.
15	Not Accessible	Not accessible (set to 0x0).

Note:

$$RThresh\Omega = \frac{(LD\_DET\_REF \times FS\_ADJ\Omega \times 18)}{(LD\_VAL \times 32)}$$

Where:

R Thresh = The threshold resistance (Ω) for load detect.

FS_ADJ = FS_ADJ resister connected to pin A2 to set current range of the A/D converters. Recommended to be 1.8 KΩ for double terminated loads (37.5 Ω), and 4 KΩ for single terminated loads (75 Ω).

LD_DET_REF = Set threshold for DAC in decimal. Refer to register 0x9E.

LD_VAL = DAC Load Value. Refer to register 0x9C.

Example: For a single terminated system (75 Ω), the following values could be used for load detection:

FS-ADJ resistor = 4 KΩ, LD_VAL = 296d, RThresh = 91 Ω, LD_DET_REF = 12.

As such, DET_DAC_A or DET_DAC_B returns a 1b if a load of ~ 91 Ω or less was detected, indicating a TV was detected.

2.2.80 I2C_DAC_LD_DET_REF - Load Detect Parameters (0x9E)

- Address Offset - 0x9Eh
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	DACB_TH$_4$	DACB_TH$_3$	DACB_TH$_2$	DACB_TH$_1$	DACB_TH$_0$	DACA_TH$_4$	DACA_TH$_3$	DACA_TH$_2$	DACA_TH$_1$	DACA_TH$_0$

Bits	Name	Description
4:0	DACA_TH[4:0]	Set threshold for DAC A load detection. 5-bit resolution, but guarantees 4-bit resolution.
9:5	DACB_TH[4:0]	Set threshold for DAC B load detection. 5-bit resolution, but guarantees 4-bit resolution.
15:10	Not Accessible	Not accessible (set to 0x0).

2.2.81 I2C_DAC_CNTL - DAC Control Parameters (0xA0)

- Address Offset - 0xA0
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC_DCRB	DAC_DCRA	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	DAC_BMUX_2	Not Accessible	DAC_AMUX_0

Bits	Name	Description
0	DAC_AMUX	**DAC A Output Mux.** Refer to Table 2-6 for functionality.
1	Not Accessible	Not accessible (set to 0x0).
2	DAC_BMUX	**DAC B Output Mux.** Refer to Table 2-6 for functionality.
13:3	Not Accessible	Not accessible (set to 0x0).
14	DAC_DCRA	**DAC A DCR.** Enable DC restore.
15	DAC_DCRB	**DAC B DCR.** Enable DC restore.

2.2.82 2C_RED_MTX_COEF - RGB to YCrCb Red Coefficient (0xA2)

- Address Offset - 0xA2
- Default Value - 0x004D
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	RED_MTX_7	RED_MTX_6	RED_MTX_5	RED_MTX_4	RED_MTX_3	RED_MTX_2	RED_MTX_1	RED_MTX_0

Bits	Name	Description
7:0	RED_MTX[7:0]	**RGB to YCrCb Matrix Red Coefficient**. Refer to the matrix in the Video Control register entry (Section 2.2.31) and Table 2.9 for values of the coefficients.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.83 I2C_GRN_MTX_COEF - RGB to YCrCb Green Coefficient (0xA4)

- Address Offset - 0xA4
- Default Value - 0x0096
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	GRN_MTX_7	GRN_MTX_6	GRN_MTX_5	GRN_MTX_4	GRN_MTX_3	GRN_MTX_2	GRN_MTX_1	GRN_MTX_0

Bits	Name	Description
7:0	GRN_MTX[7:0]	**RGB to YCrCb Matrix Green Coefficient**. See the matrix in the Video Control register entry (Section 2.2.31) and Table 2.9 for values of the coefficients.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.84 I2C_BLU_MATRIX_COEF - RGB to YCrCb Blue Coefficient (0xA6)

- Address Offset - 0xA6
- Default Value - 0x001D
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	BLU_MTX_7	BLU_MTX_6	BLU_MTX_5	BLU_MTX_4	BLU_MTX_3	BLU_MTX_2	BLU_MTX_1	BLU_MTX_0

Bits	Name	Description
7:0	BLU_MTX[7:0]	**RGB to YCrCb Matrix Blue Coefficient**. See the matrix in the Video Control register entry (Section 2.2.31) and Table 2.9 for values of the coefficients.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.85 I2C_RV_SCALE_COEF - RGB to YCrCb Red Scaling Coefficient (0xA8)

- Address Offset - 0xA8
- Default Value - 0x00A0
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	RED_SCL_8	RED_SCL_7	RED_SCL_6	RED_SCL_5	RED_SCL_4	RED_SCL_3	RED_SCL_2	RED_SCL_1	RED_SCL_0

Bits	Name	Description
8:0	RED_SCL[8:0]	**RGB to YCrCb Scaling Red Coefficient.** See the matrix in the Video Control register entry (Section 2.2.31) and Table 2.9 for values of the coefficients.
15:9	Not Accessible	Not accessible (set to 0x0).

2.2.86 I2C_GY_SCALE_COEF - RGB to YCrCb Green Scaling Coefficient (0xAA)

- Address Offset - 0xAA
- Default Value - 0x00DB
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	GRN_SCL_8	GRN_SCL_7	GRN_SCL_6	GRN_SCL_5	GRN_SCL_4	GRN_SCL_3	GRN_SCL_2	GRN_SCL_1	GRN_SCL_0

Bits	Name	Description
8:0	GRN_SCL[8:0]	**RGB to YCrCb Scaling Green Coefficient.** See the matrix in the Video Control register entry (Section 2.2.31) and Table 2.9 for values of the coefficients.
15:9	Not Accessible	Not accessible (set to 0x0).

2.2.87 I2C_BU_SCALE_COEF - RGB to YCrCb Blue Scaling Coefficient (0xAC)

- Address Offset - 0xAC
- Default Value - 0x007E
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	BLU_SCL_8	BLU_SCL_7	BLU_SCL_6	BLU_SCL_5	BLU_SCL_4	BLU_SCL_3	BLU_SCL_2	BLU_SCL_1	BLU_SCL_0

Bits	Name	Description
8:0	BLU_SCL[8:0]	**RGB to YCrCb Scaling Blue Coefficient.** See the matrix in the Video Control register entry (Section 2.2.31) and Table 2.9 for values of the coefficients.
15:9	Not Accessible	Not accessible (set to 0x0).

Table 2.9 Matrix Configurations

Video Output/ Format	Video Input	Matrix Bypass	Offset Binary	Matrix Red	Matrix Green	Matrix Blue	Scale Red (Cr)	Scale Green (Y)	Scale Blue (Cb)
NTSC (ALL)	RGB	0	--	77	150	29	160	219	126
NTSC (ALL)	YCrCb	1	1	--	--	--	256	128[1]	256
PAL (ALL)	RGB	0	--	77	150	29	160	219	126
PAL (ALL)	YCrCb	1	1	--	--	--	256	128[1]	256

1. Change green scaling coefficient to half the normal value when the offset binary bit is set.

2.2.88 I2C_CC_DATA F1 - Closed Caption Field 1 Data (0xAE)

- Address Offset - 0xAE
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC_F1_{15}	CC_F1_{14}	CC_F1_{13}	CC_F1_{12}	CC_F1_{11}	CC_F1_{10}	CC_F1_{9}	CC_F1_{8}	CC_F1_{7}	CC_F1_{6}	CC_F1_{5}	CC_F1_{4}	CC_F1_{3}	CC_F1_{2}	CC_F1_{1}	CC_F1_{0}

Bits	Name	Description
15:0	CC_F1[15:0]	**Closed Captioning Field 1.** Contains the 16-bit value to write in the next NTSC field 1 (odd field) closed caption line. Returns zero when a value has been written. Note that the closed caption specification dictates what value should appear in which field. In PAL, values written to this register appear in PAL field 2 (odd field).

2.2.89 I2C_CC_DATA_F2 - Closed Caption Field 2 Data (0xB0)

Address Offset - 0xB0

Default Value - 0x0000

Attribute - R/W

Size - 16 bits

Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC_F2_{15}	CC_F2_{14}	CC_F2_{13}	CC_F2_{12}	CC_F2_{11}	CC_F2_{10}	CC_F2_9	CC_F2_8	CC_F2_7	CC_F2_6	CC_F2_5	CC_F2_4	CC_F2_3	CC_F2_2	CC_F2_1	CC_F2_0

Bits	Name	Description
15:0	CC_F2[15:0]	**Closed Captioning Field 2.** Contains the 16-bit value to write in the next NTSC field 2 (even field) closed caption line. Returns zero when the value has been written. Note that the closed caption specification dictates what value should appear in which field. In PAL, values written to this register appear in PAL field 1 (even field).

2.2.90 I2C_CC_CNTL - Closed Caption Control (0xB2)

- Address Offset 0xB2
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC_EN_F2	CC_EN_F1	CC_LEVEL	EPARITY	$F2\_LOS_5$	$F2\_LOS_4$	$F2\_LOS_3$	$F2\_LOS_2$	$F2\_LOS_1$	$F2\_LOS_0$	$F1\_LOS_5$	$F1\_LOS_4$	$F1\_LOS_3$	$F1\_LOS_2$	$F1\_LOS_1$	$F1\_LOS_0$

Bits	Name	Description
5:0	F1_LOS[5:0]	**F1 CC Line Offset.** Selects the Field 1 Closed Caption line number.
11:6	F2_LOS[5:0]	**F2 CC Line Offset.** Selects the Field 2 Closed Caption line number.
12	EPARITY	**Even Parity.** If set parity of the CC data sent will be even, if clear parity will be odd. Parity of input CC data is ignored.
13	CC_LEVEL	**TBD.**
14	CC_EN_F1	**CC Enable Field 1.** If set enables the Closed Caption for Field 1.
15	CC_EN_F2	**CC Enable Field 2.** If set enables the Closed Caption for Field 2.

2.2.91 I2C_CC_BLNK - Closed Caption Blanking Value (0xB4)

- Address Offset - 0xB4
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	YC_BLNK_7	YC_BLNK_6	YC_BLNK_5	YC_BLNK_4	YC_BLNK_3	YC_BLNK_2	YC_BLNK_1	YC_BLNKS_0

Bits	Name	Description
7:0	YC_BLNK[9:0]	**YC CC Blanking Value.** 8-bit closed caption luma blanking value. Set to zero for automatic.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.92 I2C_CC_SHT - Closed Caption Blanking Sample (0xB6)

- Address Offset - 0xB6
- Default Value - 0x00F0
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	CC_BKS_9	CC_BKS_8	CC_BKS_7	CC_BKS_6	CC_BKS_5	CC_BKS_4	CC_BKS_3	CC_BKS_2	CC_BKS_1	CC_BKS_0

Bits	Name	Description
9:0	CC_BKS[9:0]	**CC Blanking Sample Value.** Sets the horizontal position where the closed caption signal begins to be multiplexed in. If the closed caption blanking value is zero, then the output value at the blanking sample point is also used for the CC blanking value.
15:10	Not Accessible	Not accessible (set to 0x0).

2.2.93 Not Accessible (0xB8)

2.2.94 Not Accessible (0xBA)

2.2.95 Not Accessible (0xBC)

2.2.96 Not Accessible (0xBE)

2.2.97 Not Accessible (0xC0)

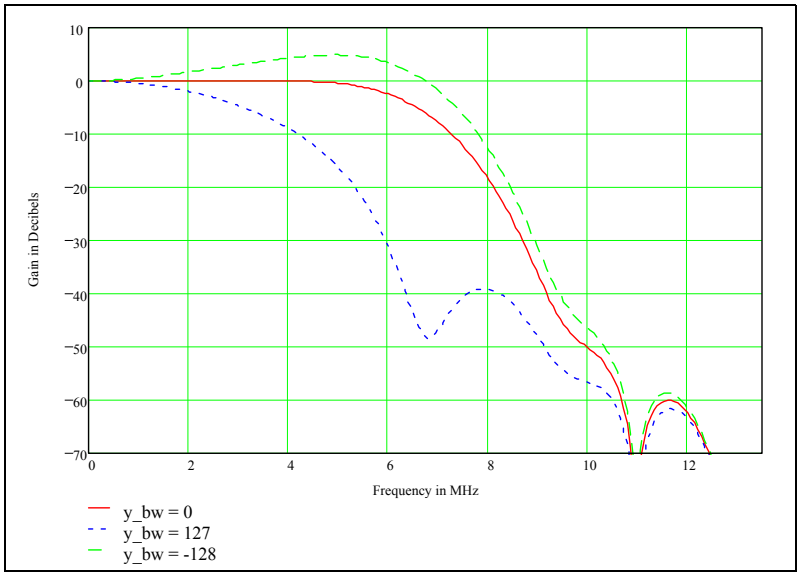
2.2.98 I2C_LUMA_BW_COEF - Luma Bandwidth (0xC2)

- Address Offset - 0xC2
- Default Value - 0x0000
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Y_BW_7	Y_BW_6	Y_BW_5	Y_BW_4	Y_BW_3	Y_BW_2	Y_BW_1	Y_BW_0

Bits	Name	Description
7:0	Y_BW[7:0]	**Luma Bandwidth.** 2's complement value attenuates or amplifies the high frequency response. Y_BW = 0 for flat response, Y_BW = 127 for 10 dB of cut, and Y_BW = -128 for 5dB of boost.
15:8	Not Accessible	Not accessible (set to 0x0).

Figure 3 Luminance Frequency Response



2.2.99 (0xC4) Reserved

2.2.100 I2C_PDIV - PLL Pre-Divider (0xC6)

- Address Offset - 0xC6
- Default Value - 0x0114
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	P_PCLK	P_DIV_7	P_DIV_6	P_DIV_5	P_DIV_4	P_DIV_3	P_DIV_2	P_DIV_1	P_DIV_0

Bits	Name	Description
7:0	P_DIV[7:0]	**PLL Pre-Divider.** Divides incoming clock by N+1. Set to N from 1 through 255 for division by 2 through 256. Set to N=0 for pass through mode. Refer to the frequency requirements in Table 2.11
8	P_PCLK	**PCLK Select.** Set to supply PLL clock from external PCLK; clear to supply PLL with external OSC clock.
15:9	Not Accessible	Not accessible (set to 0x0).

2.2.101 I2C_PLL_AMP - PLL AMP - Main PLL Divider (0xC8)

- Address Offset - 0xC8
- Default Value - 0x012C
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	$PLLICP_2$	$PLLICP_1$	$PLLICP_0$	$PLLM_9$	$PLLM_8$	$PLLM_7$	$PLLM_6$	$PLLM_5$	$PLLM_4$	$PLLM_3$	$PLLM_2$	$PLLM_1$	$PLLM_0$	$PLLS_1$	$PLLS_0$

Bits	Name	Description
1:0	PLLS[1:0]	**PLL S Divider.** PLL VCO divider value such that Fvco = (M+9)*Fin*2*(S+1). Fvco must be 200-600 MHz. S must not exceed 0-3. Refer to Section 2.2.105 for the PLL programming overview. **Note:** Recommend selecting S values such that Fvco approaches 600 MHz to reduce jitter.
11:2	PLLM[9:0]	**PLL M Divider.** PLL divider value such that Fout = (M+9)*Fin. Fin must be 500 KHz-1.3 MHz. Fout must be 100-300 MHz. M must not exceed 10-2040. Refer to Section 2.2.105 for the PLL programming overview.
14:12	PLLICP[2:0]	**Charge Pump Gain.** Sets the current for the charge pump. Please contact your Focus Enhancements FAE for value.
15	Not Accessible	Not accessible (set to 0x0).

2.2.102 I2C_PLL_VGA - PLL VGA Clock Post Divider (0xCA)

- Address Offset - 0xCA
- Default Value - 0x0003
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	VGA_P_CLK	P_VGA$_6$	P_VGA$_5$	P_VGA$_4$	P_VGA$_3$	P_VGA$_2$	P_VGA$_1$	P_VGA$_0$

Bits	Name	Description
6:0	P_VGA[6:0]	**PLL VGA Post Divider.** Divides the incoming clock by N+1. Set N from 1 through 127 for division by 2 through 128. Set to N=0 for pass-through mode. Note that this divider is used only in special cases.
7	VGA_P_CLK	**PCLK Select.** Set this bit to supply the internal VGA clock directly from the external PCLK. Clear this bit to supply with a PLL generated clock from the VGA post divider.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.103 I2C_PLL_TV - PLL TV Clock Post Divider (0xCC)

- Address Offset - 0xCC
- Default Value - 0x0003
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	TV_P_CLK	TV_OSC	P_TV_6	P_TV_5	P_TV_4	P_TV_3	P_TV_2	P_TV_1	P_TV_0

Bits	Name	Description
6:0	P_TV[6:0]	**PLL TV Post Divider.** Divides the incoming clock by N+1. Set to N from 1 through 127 for division by 2 through 128. Set to N = 0 for pass through mode.
7	TV_OSC	**OSC Select.** Set to supply the internal TV clock from PLL generated clock from TV post divider or PCLK; clear to supply directly from the external oscillator. Refer to the bit 8 definition in Table 2.10 for TV_P_PCLK dependency.
8	TV_P_CLK	**PCLK Select.** Set to supply the internal TV clock directly from external PCLK; clear to supply with PLL generated clock from TV post divider. Refer to bit 7 in Table 2.10 for TV_OSC dependency.
15:9	Not Accessible	Not accessible (set to 0x0).

Table 2.10 Internal TV Clock Selection

TV_P_CLK Bit 8	TV_OSC Bit 7	Internal TV Clock Equals
0b	0b	Ext. OSC
0b	1b	TV Post Divider
1b	0b	Ext. OSC
1b	1b	PCLK

2.2.104 I2C_PLL_GCC - PLL GCC Clock Post Divider (0xCE)

- Address Offset - 0xCE
- Default Value - 0x0003
- Attribute - R/W
- Size - 16 bits
- Allowed Range - N/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	Not Accessible	XTAL_OUT	P_GCC_6	P_GCC_5	P_GCC_4	P_GCC_3	P_GCC_2	P_GCC_1	P_GCC_0

Bits	Name	Description
6:0	P_GCC[6:0]	**PLL GCC Post Divider.** Divides the incoming clock by N+1. Set to N from 1 through 127 for division by 2 through 128. Set to N = 0 for pass through mode.
7	XTAL_OUT	**XTAL Output.** Set to 0b to route the XTAL to the GCC clock output. Set to 1b for PLL sources.
15:8	Not Accessible	Not accessible (set to 0x0).

2.2.105 Notes for PLL Registers (0xC6, 0xC8, 0xCA, 0xCC, 0xCE)

In master mode, the FS471 synthesizes a 2.5 MHz to 85 MHz clock from a 2.5 MHz to 35 MHz crystal and supplies this clock (CLKOUT) to the GCC. The clock is buffered and returned to the FS471 as a Pixel Clock (PCLK) synchronous to the pixel and sync data.

In slave mode, the FS471 synthesizes a 2.5 MHz to 85 MHz clock from a 2.5 MHz - 85 MHz pixel clock.

Allow for a 100 µs PLL settling when changing PLL settings.

Figure 4 FS47x Block Diagram

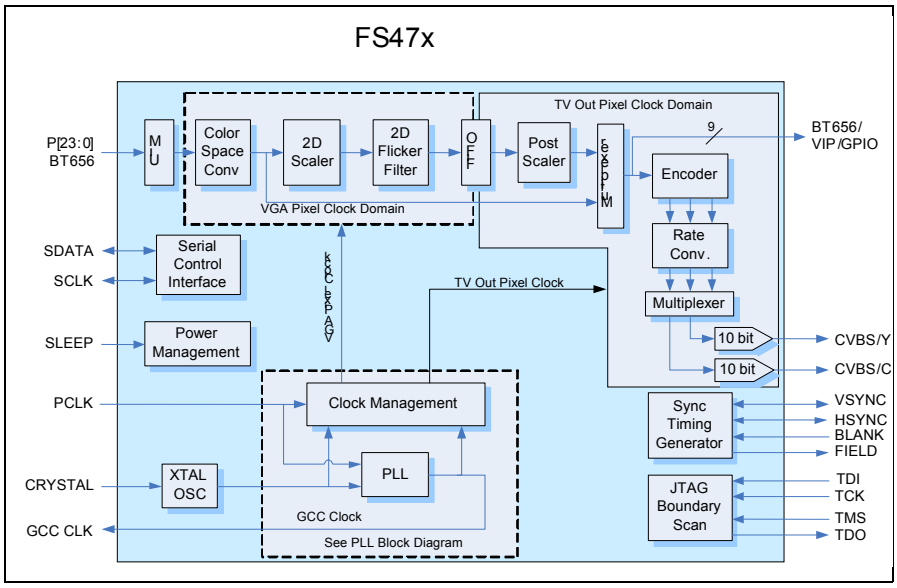
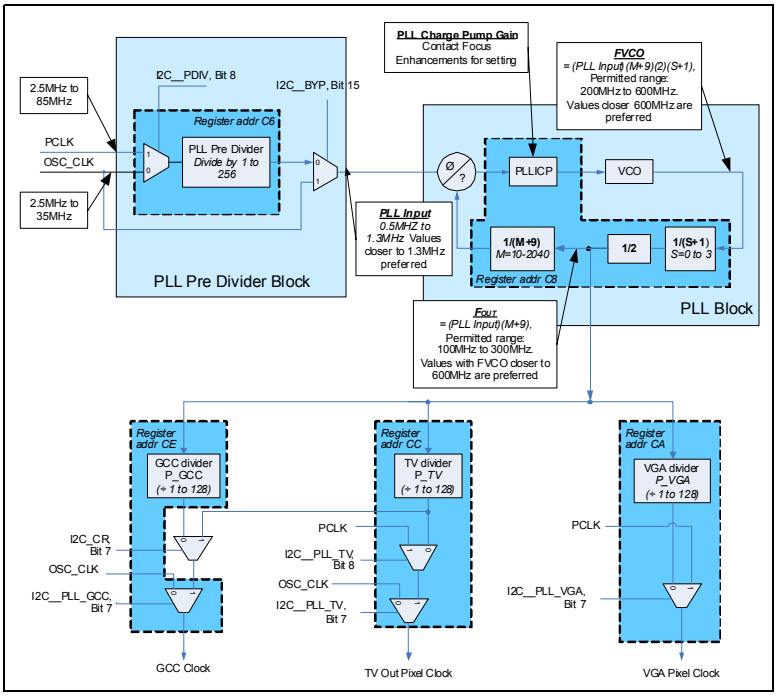


Figure 5 PLL Block Diagram



Note: *Refer to the PLL frequency limits in Table 2.11.*